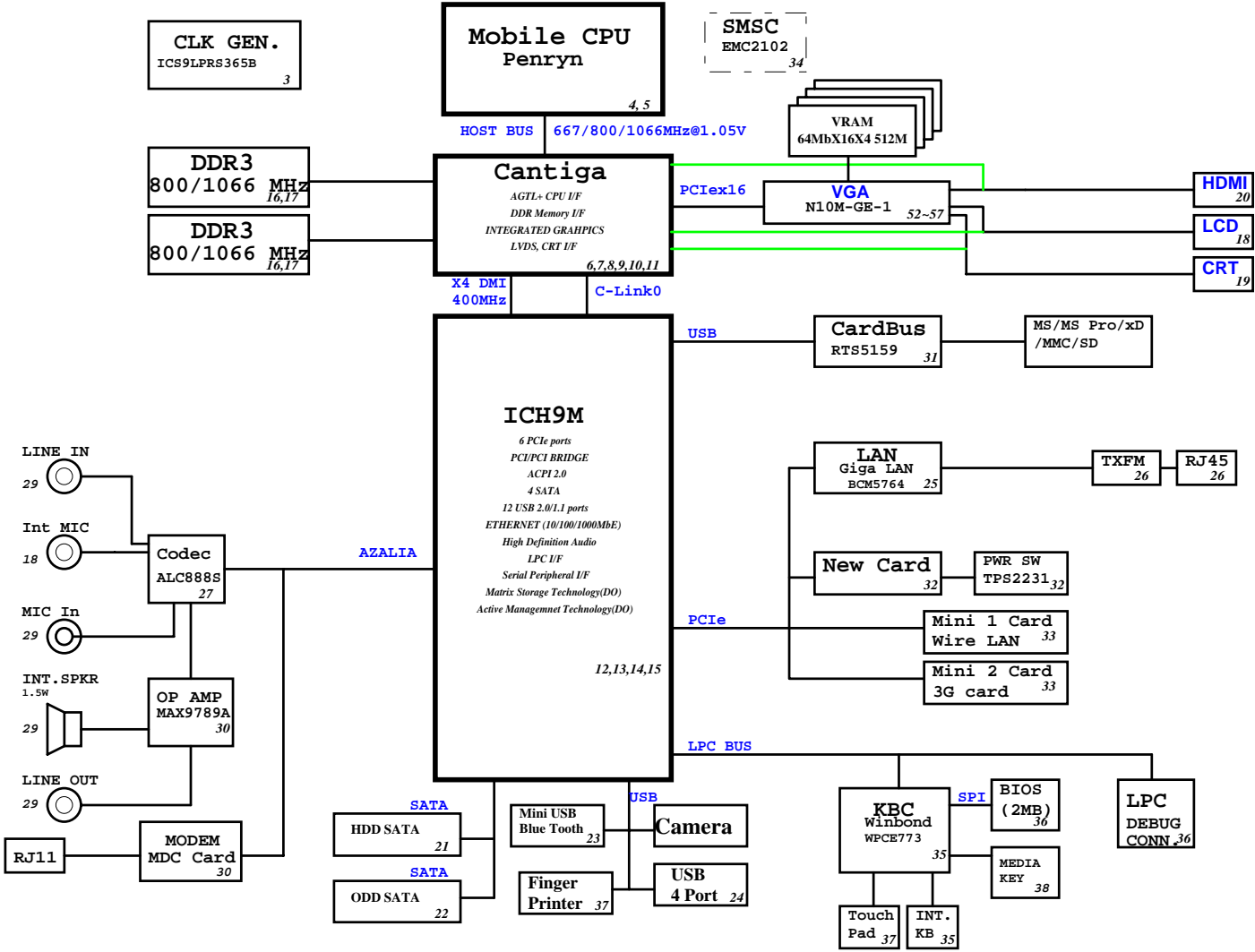


JV50 Block Diagram

Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP

TOP	_____	L1
GND	_____	L2
S	_____	L3
S	_____	L4
GND	_____	L5
BOTTOM	_____	L6

SYSTEM DC/DC	
ISL62392	42
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC	
TPS51124	43
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)
RT9026	44
1D5V_S3	DDR_VREF_S3(1.2A)
RT9018	44
1D5V_S3	1D1V_S0(2A)
TPS51117	45
DCBATOUT	FBVDD(4A)
CHARGER	
ISL88731A	47
INPUTS	OUTPUTS
DCBATOUT	BT+
CPU DC/DC	
ISL6266A	41
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A
VGA_CORE	
RT8202A	47
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A
GFXCORE	
ISL6263A	46
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

JV50

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

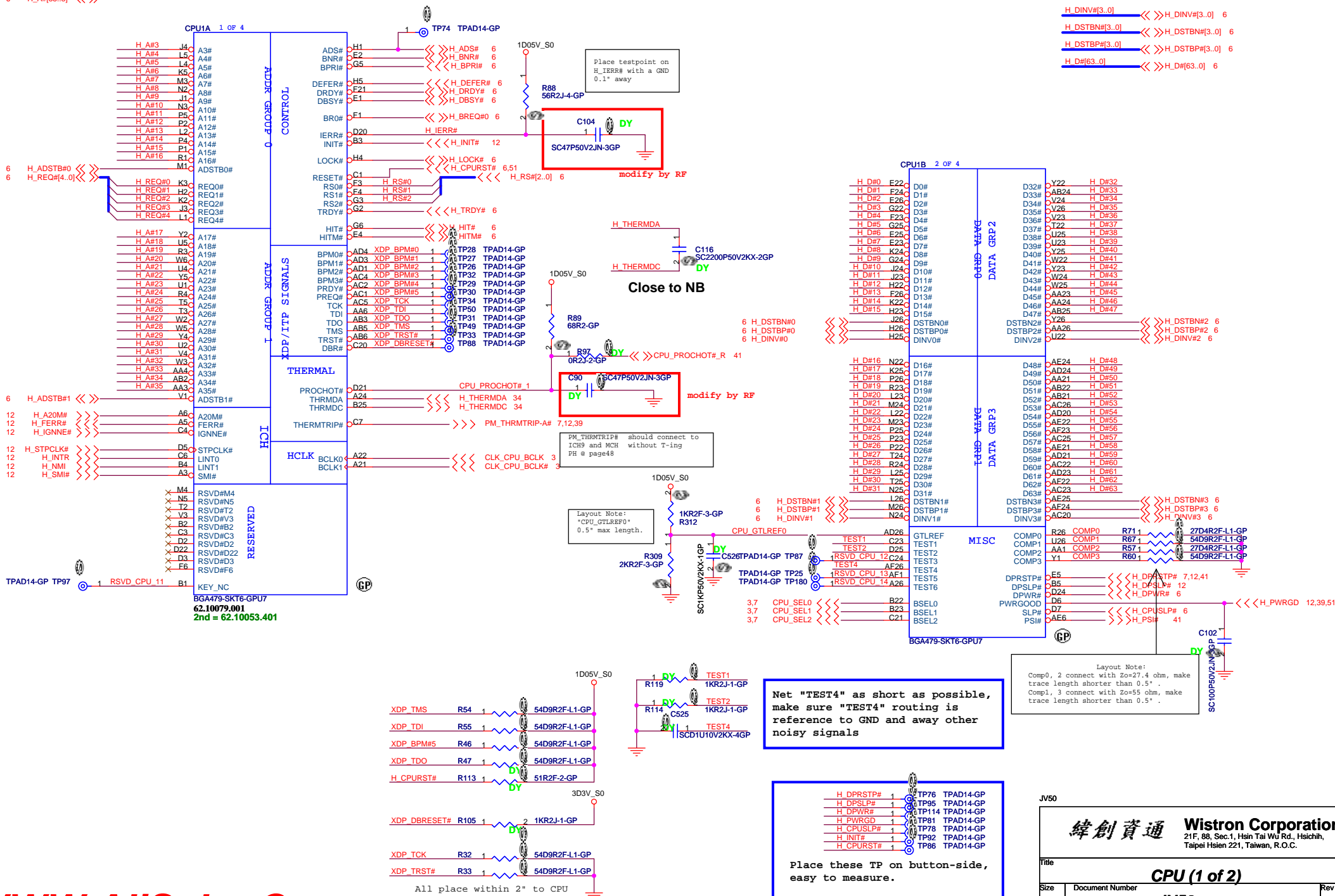
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

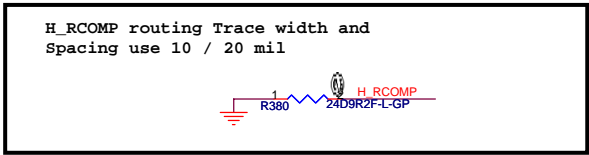
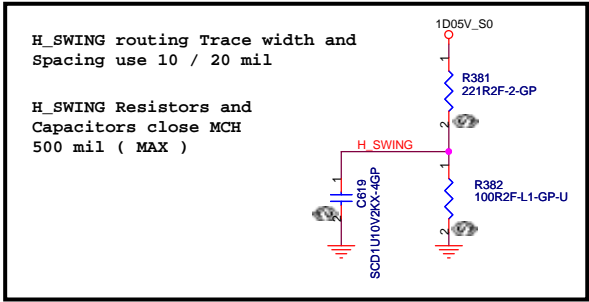
NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

JV50

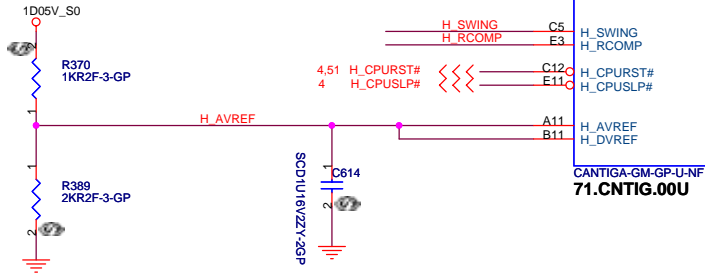
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	Rev	SB
JV50			
Date: Tuesday, December 16, 2008			
Sheet 2		of 60	

6 H_A#(35..3) <<< H_A#(35..3)





Place them near to the chip (< 0.5")



NB1A		1 OF 10	
H_D#0	F2	H_A#_3	A14
H_D#1	G8	H_A#_4	C15
H_D#2	F8	H_A#_5	F16
H_D#3	F6	H_A#_6	H13
H_D#4	G2	H_A#_7	C18
H_D#5	H6	H_A#_8	M16
H_D#6	F2	H_A#_9	J13
H_D#7	D4	H_A#_10	P16
H_D#8	H3	H_A#_11	R16
H_D#9	M9	H_A#_12	N17
H_D#10	M11	H_A#_13	M13
H_D#11	J2	H_A#_14	E17
H_D#12	N12	H_A#_15	P17
H_D#13	J6	H_A#_16	E17
H_D#14	L2	H_A#_17	G20
H_D#15	P2	H_A#_18	B19
H_D#16	N9	H_A#_19	J16
H_D#17	L6	H_A#_20	E20
H_D#18	M5	H_A#_21	H16
H_D#19	J3	H_A#_22	J20
H_D#20	N2	H_A#_23	L17
H_D#21	R1	H_A#_24	A17
H_D#22	N5	H_A#_25	B17
H_D#23	N6	H_A#_26	L16
H_D#24	P13	H_A#_27	C21
H_D#25	N8	H_A#_28	J17
H_D#26	L7	H_A#_29	H20
H_D#27	N10	H_A#_30	K17
H_D#28	M3	H_A#_31	B20
H_D#29	Y3	H_A#_32	F21
H_D#30	Y6	H_A#_33	K21
H_D#31	Y10	H_A#_34	L20
H_D#32	Y12	H_A#_35	
H_D#33	Y14		
H_D#34	Y2		
H_D#35	AA8		
H_D#36	Y9		
H_D#37	AA13		
H_D#38	AA9		
H_D#39	AA11		
H_D#40	AD11		
H_D#41	AD10		
H_D#42	AD13		
H_D#43	AE12		
H_D#44	AE9		
H_D#45	AA2		
H_D#46	AD8		
H_D#47	AD3		
H_D#48	AE3		
H_D#49	AC3		
H_D#50	AE11		
H_D#51	AE8		
H_D#52	AG2		
H_D#53	AD6		

ISOH

H_A#_3	A14	H_A#3	H_A#35.3]
H_A#_4	C15	H_A#4	H_A#35.3]
H_A#_5	F16	H_A#5	H_A#35.3]
H_A#_6	H13	H_A#6	H_A#35.3]
H_A#_7	C18	H_A#7	H_A#35.3]
H_A#_8	M16	H_A#8	H_A#35.3]
H_A#_9	J13	H_A#9	H_A#35.3]
H_A#_10	P16	H_A#10	H_A#35.3]
H_A#_11	R16	H_A#11	H_A#35.3]
H_A#_12	N17	H_A#12	H_A#35.3]
H_A#_13	M13	H_A#13	H_A#35.3]
H_A#_14	E17	H_A#14	H_A#35.3]
H_A#_15	P17	H_A#15	H_A#35.3]
H_A#_16	E17	H_A#16	H_A#35.3]
H_A#_17	G20	H_A#17	H_A#35.3]
H_A#_18	B19	H_A#18	H_A#35.3]
H_A#_19	J16	H_A#19	H_A#35.3]
H_A#_20	E20	H_A#20	H_A#35.3]
H_A#_21	H16	H_A#21	H_A#35.3]
H_A#_22	J20	H_A#22	H_A#35.3]
H_A#_23	L17	H_A#23	H_A#35.3]
H_A#_24	A17	H_A#24	H_A#35.3]
H_A#_25	B17	H_A#25	H_A#35.3]
H_A#_26	L16	H_A#26	H_A#35.3]
H_A#_27	C21	H_A#27	H_A#35.3]
H_A#_28	J17	H_A#28	H_A#35.3]
H_A#_29	H20	H_A#29	H_A#35.3]
H_A#_30	K17	H_A#30	H_A#35.3]
H_A#_31	B20	H_A#31	H_A#35.3]
H_A#_32	F21	H_A#32	H_A#35.3]
H_A#_33	K21	H_A#33	H_A#35.3]
H_A#_34	L20	H_A#34	H_A#35.3]
H_A#_35		H_A#35	H_A#35.3]

H_ADS#	H_ADS#	H_ADS#	H_ADS#
H_ADSTB#_0	H_ADSTB#_0	H_ADSTB#_0	H_ADSTB#_0
H_ADSTB#_1	H_ADSTB#_1	H_ADSTB#_1	H_ADSTB#_1
H_BNR#	H_BNR#	H_BNR#	H_BNR#
H_BPRI#	H_BPRI#	H_BPRI#	H_BPRI#
H_BREQ#	H_BREQ#	H_BREQ#	H_BREQ#
H_DEFER#	H_DEFER#	H_DEFER#	H_DEFER#
H_DBSY#	H_DBSY#	H_DBSY#	H_DBSY#
HPLL_CLK#	HPLL_CLK#	HPLL_CLK#	HPLL_CLK#
HPLL_CLK#	HPLL_CLK#	HPLL_CLK#	HPLL_CLK#
H_DPWR#	H_DPWR#	H_DPWR#	H_DPWR#
H_DRDY#	H_DRDY#	H_DRDY#	H_DRDY#
H_HIT#	H_HIT#	H_HIT#	H_HIT#
H_HITM#	H_HITM#	H_HITM#	H_HITM#
H_LOCK#	H_LOCK#	H_LOCK#	H_LOCK#
H_TRDY#	H_TRDY#	H_TRDY#	H_TRDY#

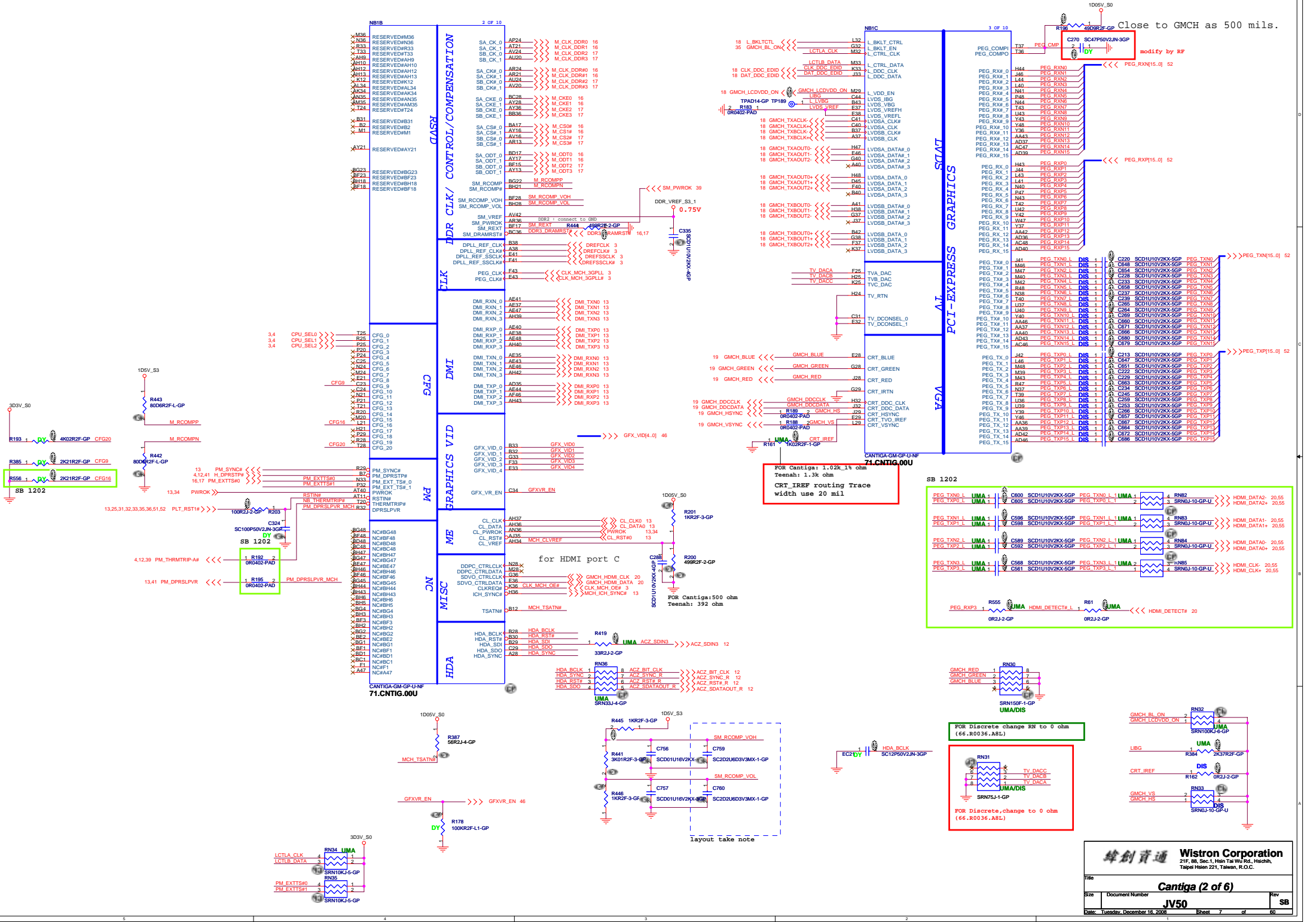
H_DINV#_0	H_DINV#_0	H_DINV#_0	H_DINV#_0
H_DINV#_1	H_DINV#_1	H_DINV#_1	H_DINV#_1
H_DINV#_2	H_DINV#_2	H_DINV#_2	H_DINV#_2
H_DINV#_3	H_DINV#_3	H_DINV#_3	H_DINV#_3

H_DSTBN#_0	H_DSTBN#_0	H_DSTBN#_0	H_DSTBN#_0
H_DSTBN#_1	H_DSTBN#_1	H_DSTBN#_1	H_DSTBN#_1
H_DSTBN#_2	H_DSTBN#_2	H_DSTBN#_2	H_DSTBN#_2
H_DSTBN#_3	H_DSTBN#_3	H_DSTBN#_3	H_DSTBN#_3

H_DSTBP#_0	H_DSTBP#_0	H_DSTBP#_0	H_DSTBP#_0
H_DSTBP#_1	H_DSTBP#_1	H_DSTBP#_1	H_DSTBP#_1
H_DSTBP#_2	H_DSTBP#_2	H_DSTBP#_2	H_DSTBP#_2
H_DSTBP#_3	H_DSTBP#_3	H_DSTBP#_3	H_DSTBP#_3

H_REQ#_0	H_REQ#_0	H_REQ#_0	H_REQ#_0
H_REQ#_1	H_REQ#_1	H_REQ#_1	H_REQ#_1
H_REQ#_2	H_REQ#_2	H_REQ#_2	H_REQ#_2
H_REQ#_3	H_REQ#_3	H_REQ#_3	H_REQ#_3
H_REQ#_4	H_REQ#_4	H_REQ#_4	H_REQ#_4

H_RS#_0	H_RS#_0	H_RS#_0	H_RS#_0
H_RS#_1	H_RS#_1	H_RS#_1	H_RS#_1
H_RS#_2	H_RS#_2	H_RS#_2	H_RS#_2



16 M_A_DQ[63.0] <<< M_A_DQ[63.0]

M A DQ0 AJ38 SA_DQ_0
M A DQ1 AJ41 SA_DQ_1
M A DQ2 AN38 SA_DQ_2
M A DQ3 AN38 SA_DQ_3
M A DQ4 AJ36 SA_DQ_4
M A DQ5 AJ40 SA_DQ_5
M A DQ6 AM44 SA_DQ_6
M A DQ7 AM42 SA_DQ_7
M A DQ8 AN43 SA_DQ_8
M A DQ9 AN44 SA_DQ_9
M A DQ10 AJ40 SA_DQ_10
M A DQ11 AT38 SA_DQ_11
M A DQ12 AN41 SA_DQ_12
M A DQ13 AN39 SA_DQ_13
M A DQ14 AU44 SA_DQ_14
M A DQ15 AU42 SA_DQ_15
M A DQ16 AV39 SA_DQ_16
M A DQ17 AY44 SA_DQ_17
M A DQ18 BA40 SA_DQ_18
M A DQ19 BD43 SA_DQ_19
M A DQ20 AV41 SA_DQ_20
M A DQ21 AY43 SA_DQ_21
M A DQ22 BA41 SA_DQ_22
M A DQ23 BC40 SA_DQ_23
M A DQ24 AY37 SA_DQ_24
M A DQ25 BD38 SA_DQ_25
M A DQ26 AV37 SA_DQ_26
M A DQ27 AT36 SA_DQ_27
M A DQ28 AY38 SA_DQ_28
M A DQ29 BA39 SA_DQ_29
M A DQ30 AV36 SA_DQ_30
M A DQ31 AW36 SA_DQ_31
M A DQ32 BD13 SA_DQ_32
M A DQ33 AU11 SA_DQ_33
M A DQ34 BC11 SA_DQ_34
M A DQ35 BA12 SA_DQ_35
M A DQ36 AU13 SA_DQ_36
M A DQ37 AV13 SA_DQ_37
M A DQ38 BD12 SA_DQ_38
M A DQ39 BC12 SA_DQ_39
M A DQ40 BA9 SA_DQ_40
M A DQ41 BA9 SA_DQ_41
M A DQ42 AU10 SA_DQ_42
M A DQ43 AV9 SA_DQ_43
M A DQ44 BA11 SA_DQ_44
M A DQ45 BD9 SA_DQ_45
M A DQ46 AY8 SA_DQ_46
M A DQ47 BA6 SA_DQ_47
M A DQ48 AV5 SA_DQ_48
M A DQ49 AV7 SA_DQ_49
M A DQ50 AT9 SA_DQ_50
M A DQ51 AN8 SA_DQ_51
M A DQ52 AU5 SA_DQ_52
M A DQ53 AU6 SA_DQ_53
M A DQ54 AT5 SA_DQ_54
M A DQ55 AN10 SA_DQ_55
M A DQ56 AM11 SA_DQ_56
M A DQ57 AM5 SA_DQ_57
M A DQ58 AJ9 SA_DQ_58
M A DQ59 AJ8 SA_DQ_59
M A DQ60 AN12 SA_DQ_60
M A DQ61 AM13 SA_DQ_61
M A DQ62 AJ11 SA_DQ_62
M A DQ63 AJ12 SA_DQ_63

NB1D

4 OF 10

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

DDR SYSTEM MEMORY A

M_A_BS#0 16
M_A_BS#1 16
M_A_BS#2 16
M_A_RAS# 16
M_A_CAS# 16
M_A_WE# 16

M_A_DM[7.0] >>> M_A_DM[7.0] 16

M_A_DQS[7.0] <<< M_A_DQS[7.0] 16

M_A_DQS#7.0 >>> M_A_DQS#7.0 16

M_A_A[14.0] >>> M_A_A[14.0] 16

17 M_B_DQ[63.0] <<< M_B_DQ[63.0]

M B DQ0 AK47 SB_DQ_0
M B DQ1 AH46 SB_DQ_1
M B DQ2 AP47 SB_DQ_2
M B DQ3 AP46 SB_DQ_3
M B DQ4 AJ46 SB_DQ_4
M B DQ5 AJ48 SB_DQ_5
M B DQ6 AM48 SB_DQ_6
M B DQ7 AP48 SB_DQ_7
M B DQ8 AU47 SB_DQ_8
M B DQ9 AJ46 SB_DQ_9
M B DQ10 BA48 SB_DQ_10
M B DQ11 AY48 SB_DQ_11
M B DQ12 AT47 SB_DQ_12
M B DQ13 AR47 SB_DQ_13
M B DQ14 BA47 SB_DQ_14
M B DQ15 BC47 SB_DQ_15
M B DQ16 BC46 SB_DQ_16
M B DQ17 BC44 SB_DQ_17
M B DQ18 BG43 SB_DQ_18
M B DQ19 BF43 SB_DQ_19
M B DQ20 BF45 SB_DQ_20
M B DQ21 BC41 SB_DQ_21
M B DQ22 BF40 SB_DQ_22
M B DQ23 BF41 SB_DQ_23
M B DQ24 BG38 SB_DQ_24
M B DQ25 BF38 SB_DQ_25
M B DQ26 BH35 SB_DQ_26
M B DQ27 BG35 SB_DQ_27
M B DQ28 BH40 SB_DQ_28
M B DQ29 BG38 SB_DQ_29
M B DQ30 BG34 SB_DQ_30
M B DQ31 BH34 SB_DQ_31
M B DQ32 BH14 SB_DQ_32
M B DQ33 BG12 SB_DQ_33
M B DQ34 BH11 SB_DQ_34
M B DQ35 BG8 SB_DQ_35
M B DQ36 BH12 SB_DQ_36
M B DQ37 BF11 SB_DQ_37
M B DQ38 BF8 SB_DQ_38
M B DQ39 BG7 SB_DQ_39
M B DQ40 BC5 SB_DQ_40
M B DQ41 BC6 SB_DQ_41
M B DQ42 AY1 SB_DQ_42
M B DQ43 BF6 SB_DQ_43
M B DQ44 BF5 SB_DQ_44
M B DQ45 BA1 SB_DQ_45
M B DQ46 BD3 SB_DQ_46
M B DQ47 AU2 SB_DQ_47
M B DQ48 AU3 SB_DQ_48
M B DQ49 AR3 SB_DQ_49
M B DQ50 AN2 SB_DQ_50
M B DQ51 AY2 SB_DQ_51
M B DQ52 AV1 SB_DQ_52
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M B DQ54 AR1 SB_DQ_54
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M B DQ56 AL2 SB_DQ_56
M B DQ57 AJ1 SB_DQ_57
M B DQ58 AH1 SB_DQ_58
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M B DQ60 AM3 SB_DQ_60
M B DQ61 AH3 SB_DQ_61
M B DQ62 AJ5 SB_DQ_62
M B DQ63 AJ5 SB_DQ_63

NB1E

5 OF 10

SB_BS_0
SB_BS_1
SB_BS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

DDR SYSTEM MEMORY B

M_B_BS#0 17
M_B_BS#1 17
M_B_BS#2 17
M_B_RAS# 17
M_B_CAS# 17
M_B_WE# 17

M_B_DM[7.0] >>> M_B_DM[7.0] 17

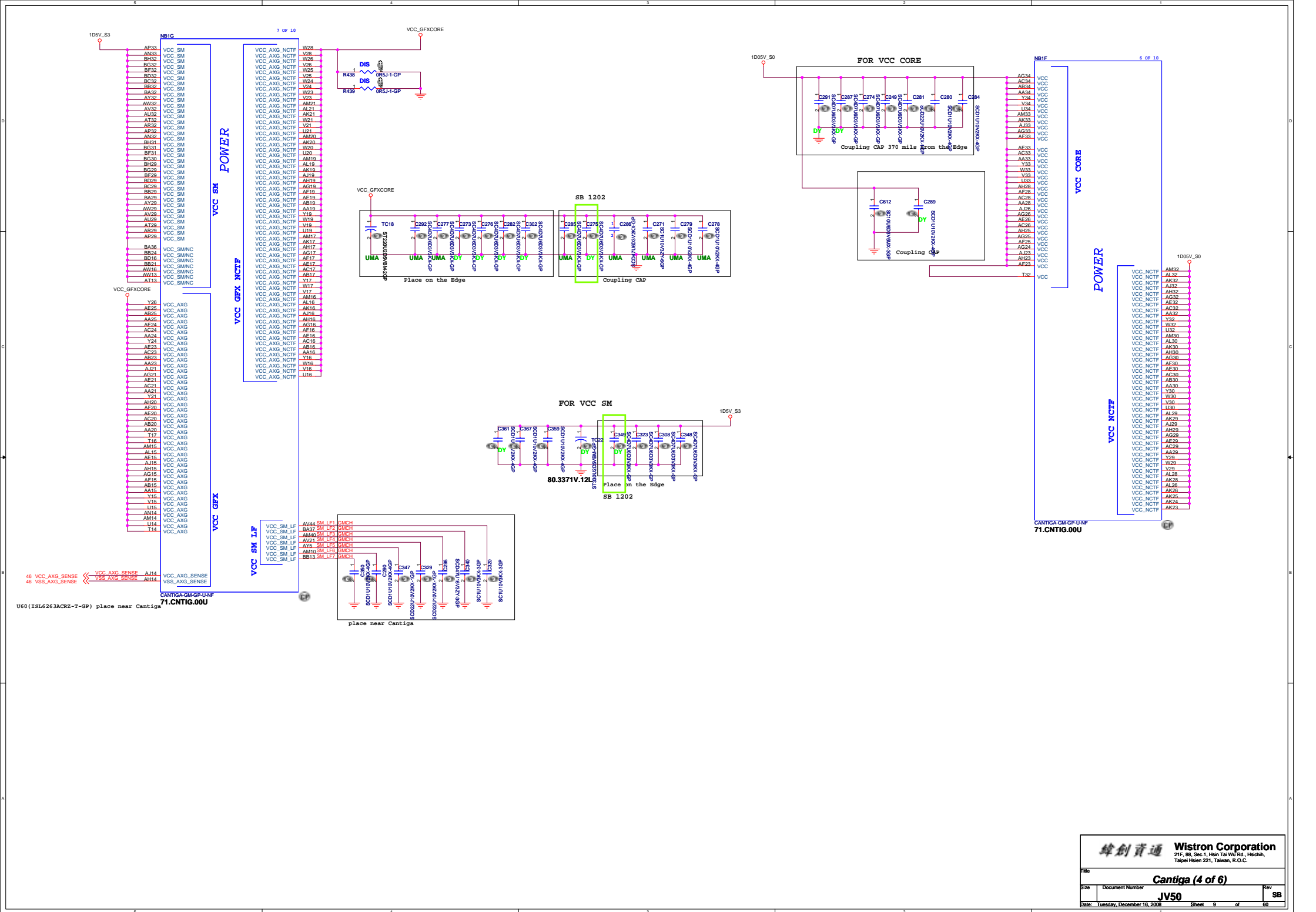
M_B_DQS[7.0] <<< M_B_DQS[7.0] 17

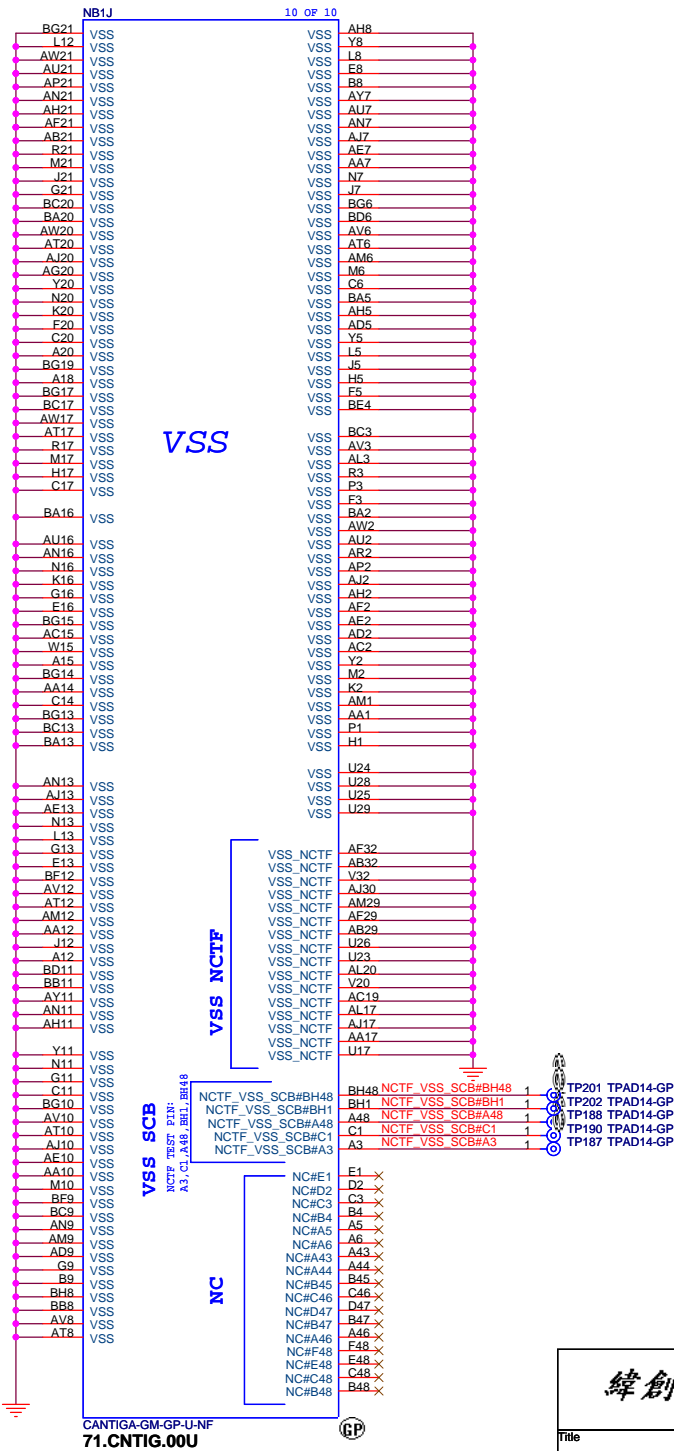
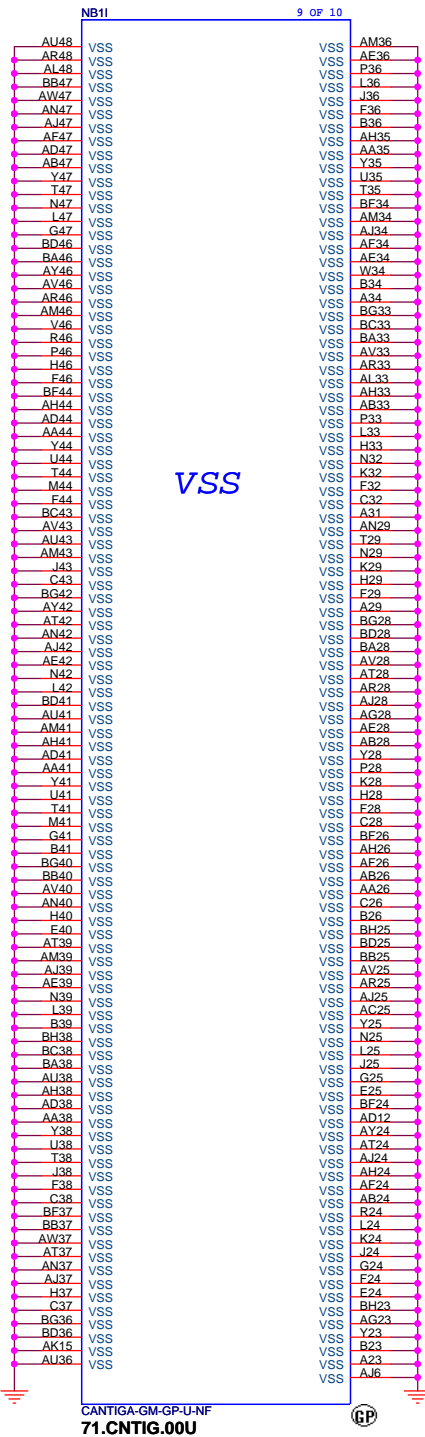
M_B_DQS#7.0 >>> M_B_DQS#7.0 17

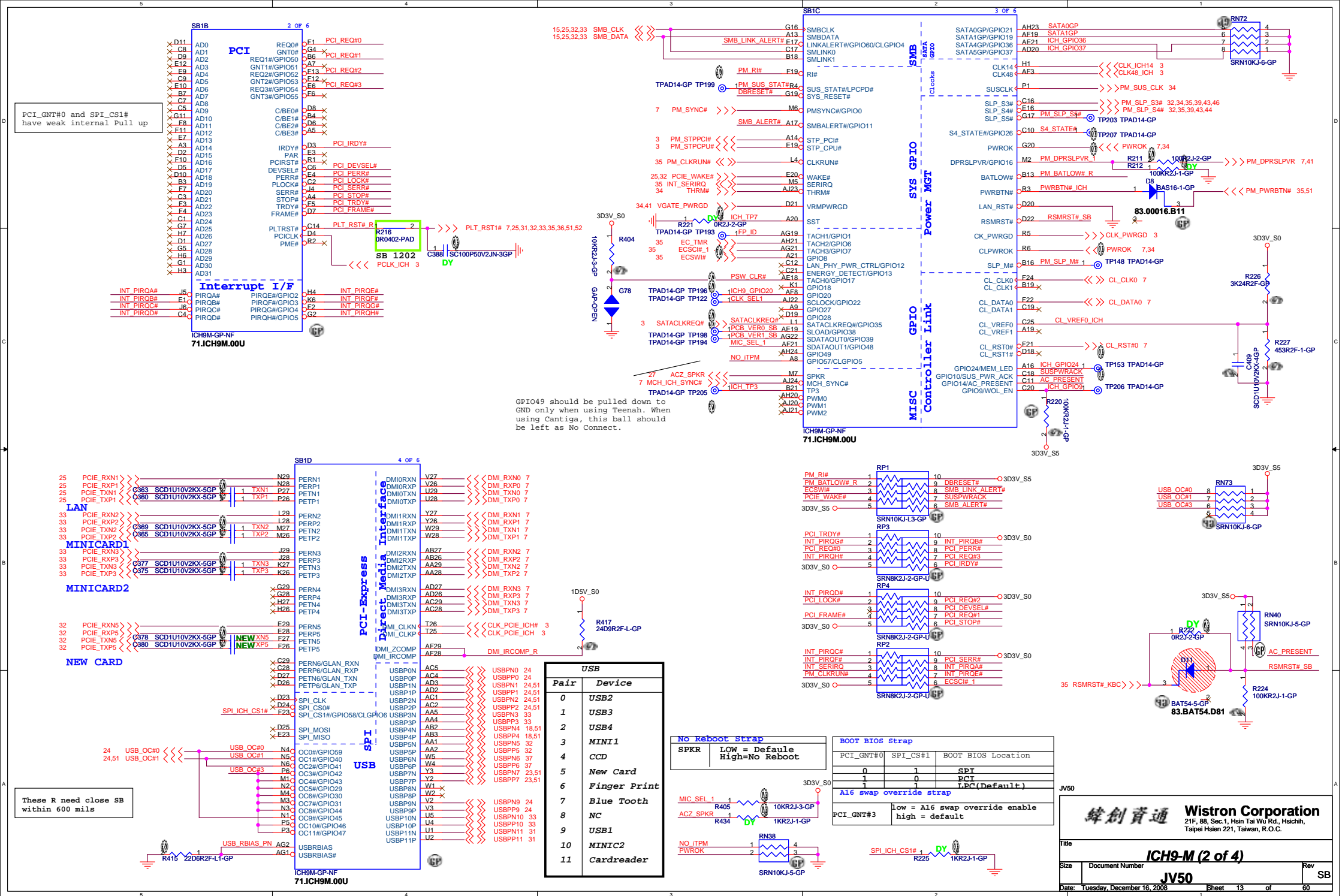
M_B_A[14.0] >>> M_B_A[14.0] 17

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Title		
Cantiga (3 of 6)		
Size	Document Number	Rev
	JV50	SB
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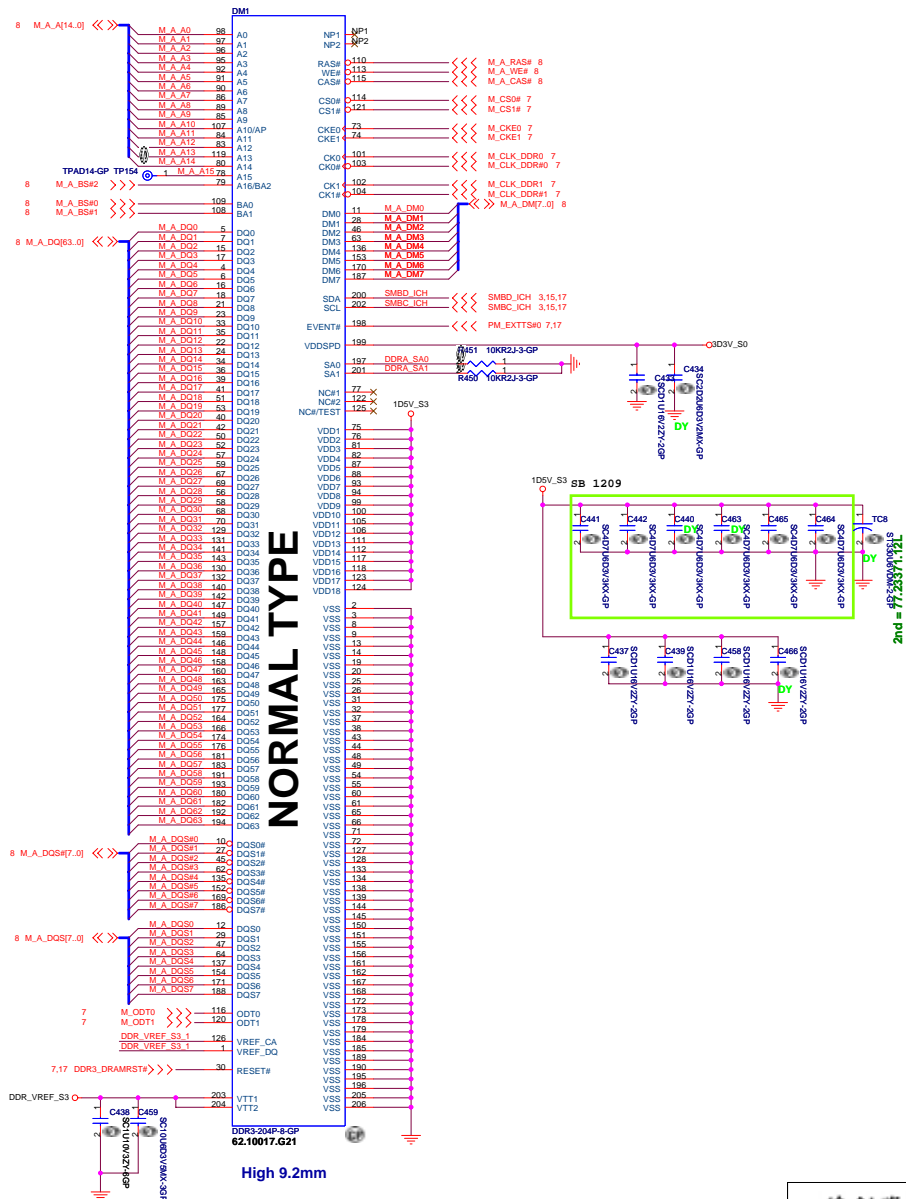




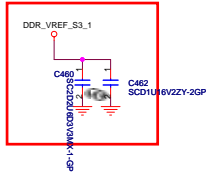




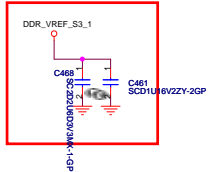
DDR3 SOCKET_1



Layout Note : Near Pin 126



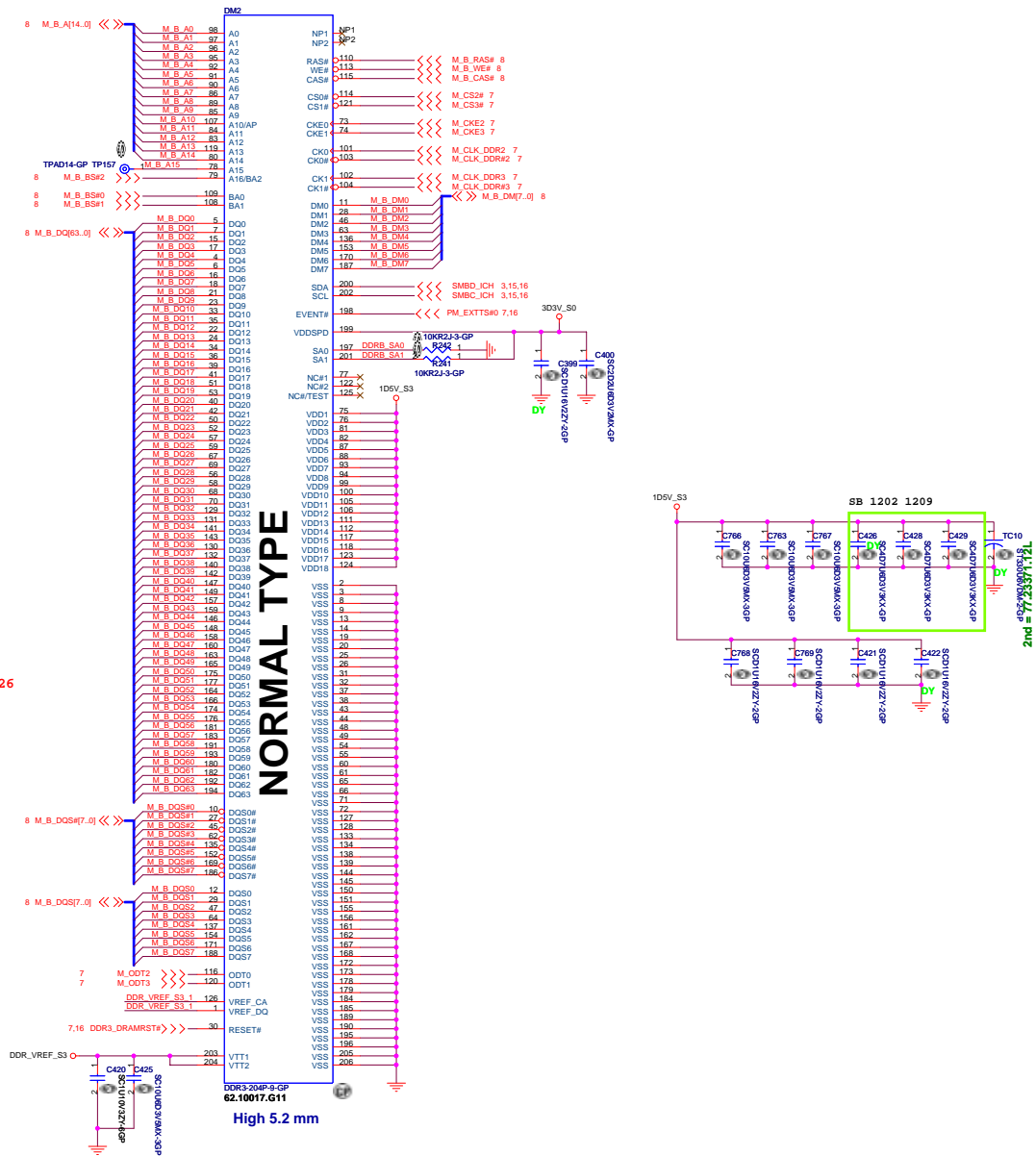
Layout Note : Near Pin 1



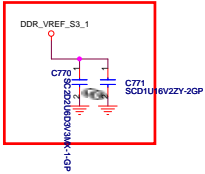
NORMAL TYPE

2n.

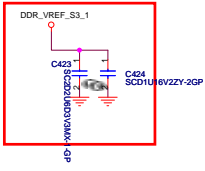
DDR3 SOCKET_2



Layout Note : Near Pin 126



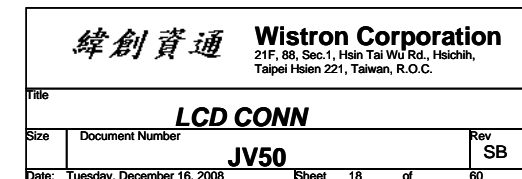
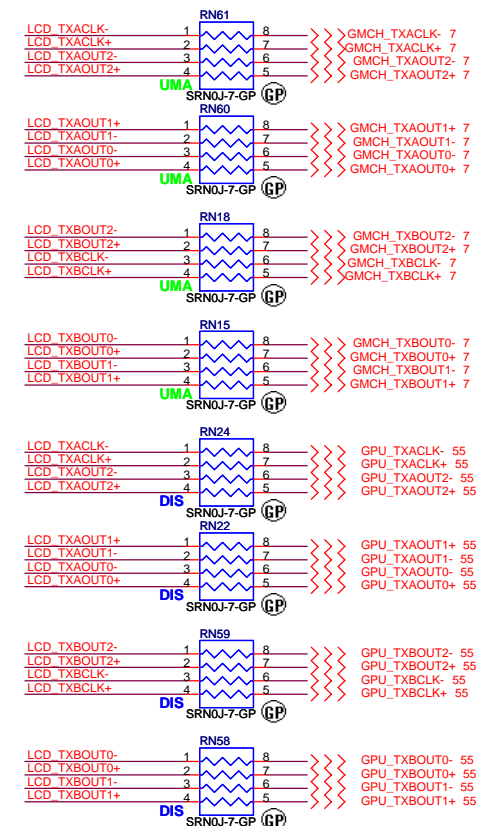
Layout Note : Near Pin 1



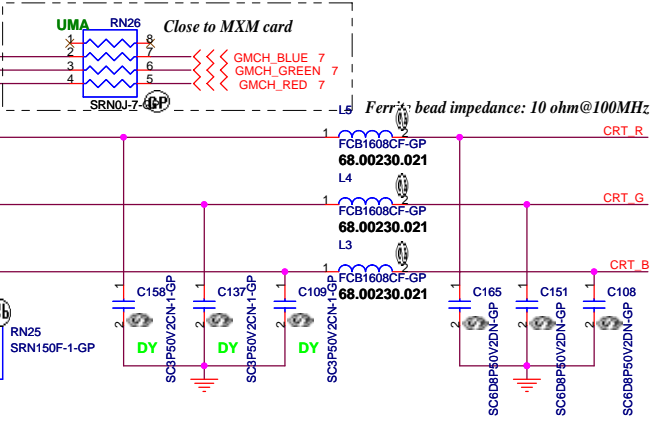
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
DDR3 Socket2			
Size	Document Number	Rev	SB
	JV50		
Date: Tuesday, December 18, 2008	Sheet	17	of 60

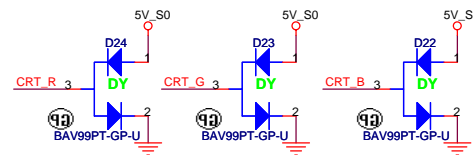
WWW.AliSaler.Com



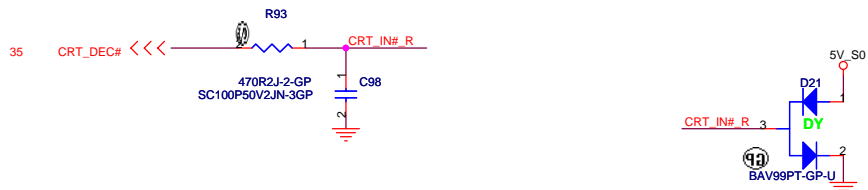
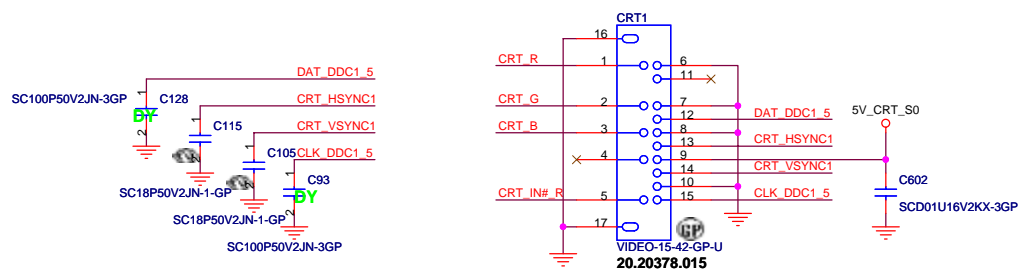
Layout Note:
Place these resistors
close to the CRT-out
connector



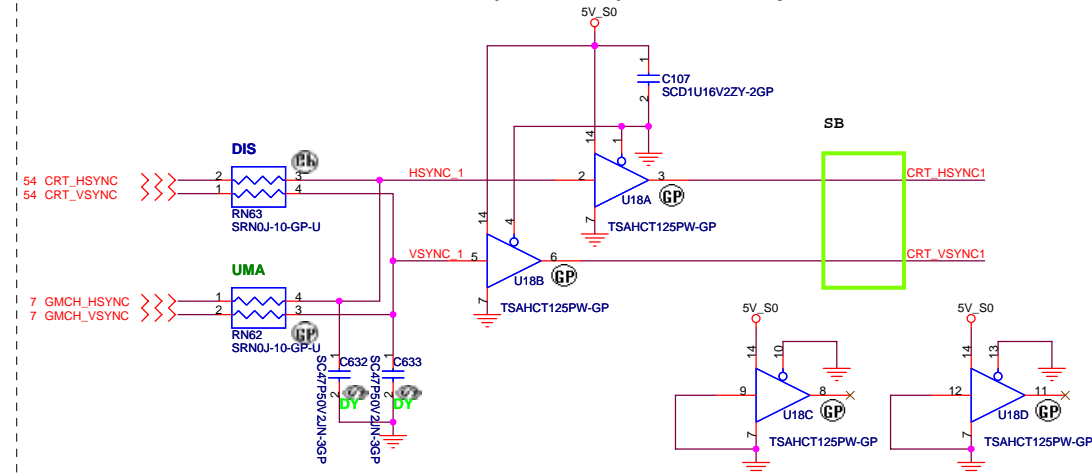
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



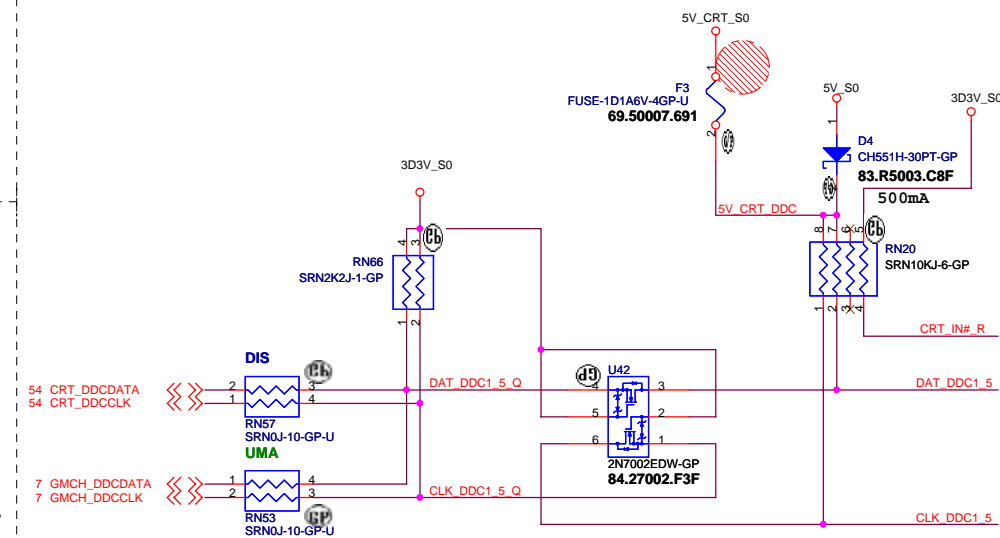
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



JV50

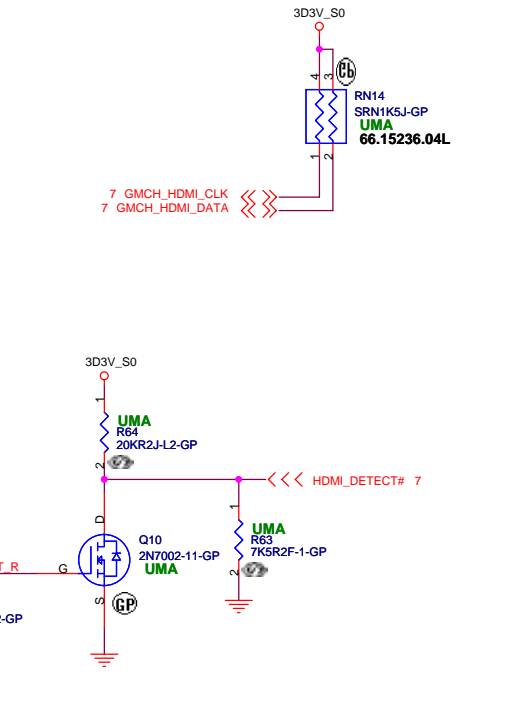
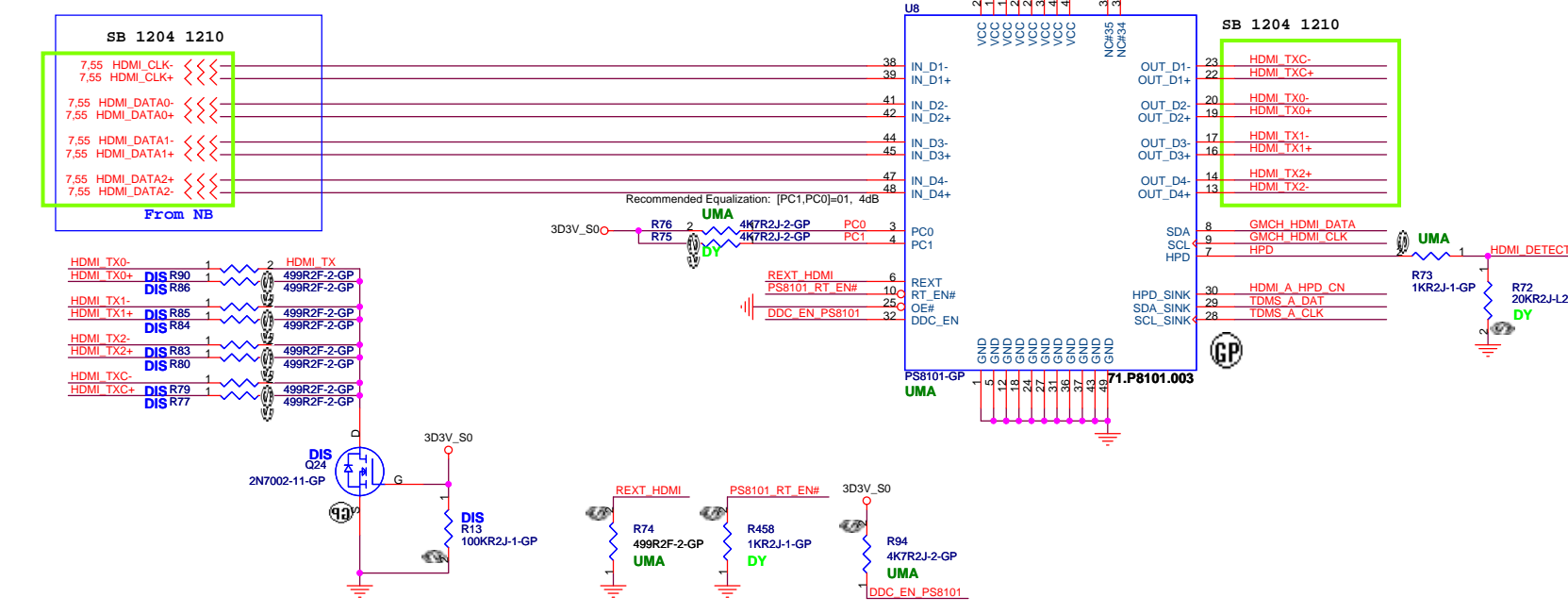
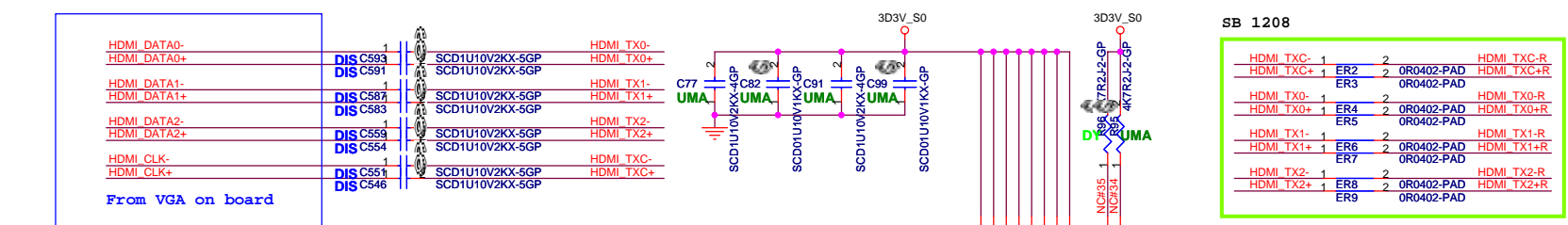
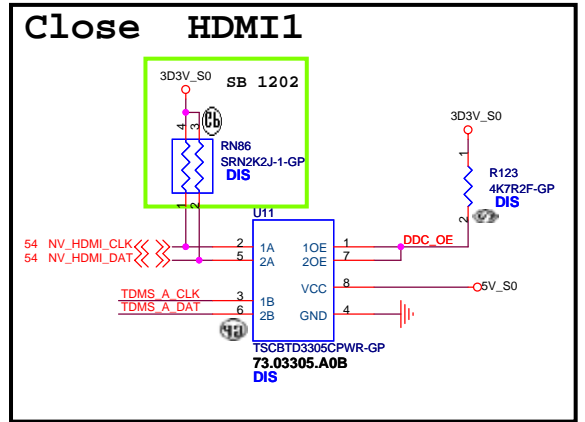
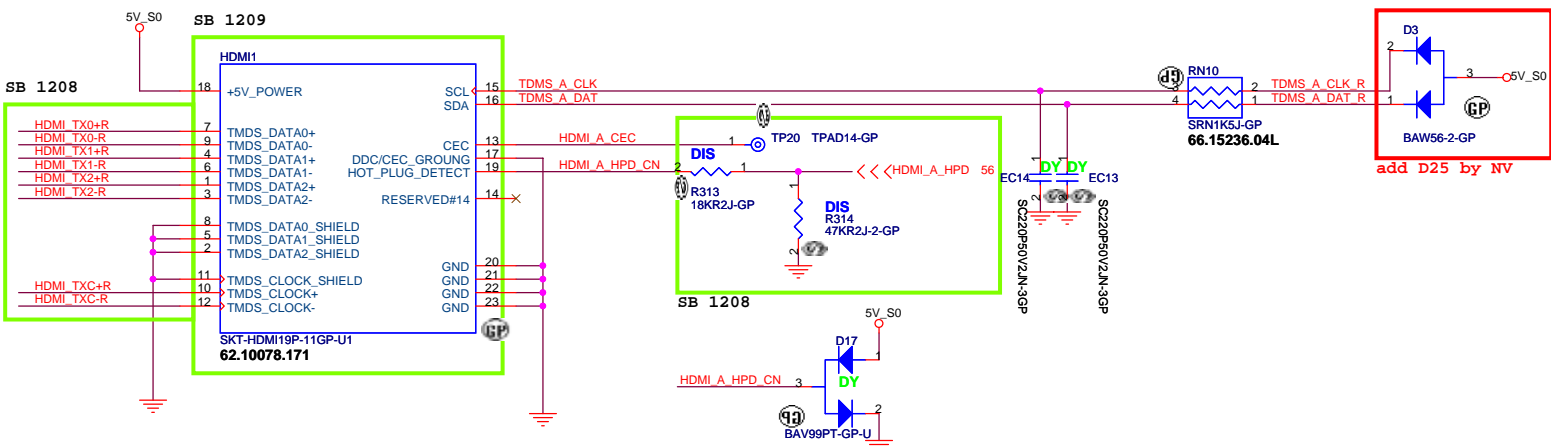
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Size Document Number
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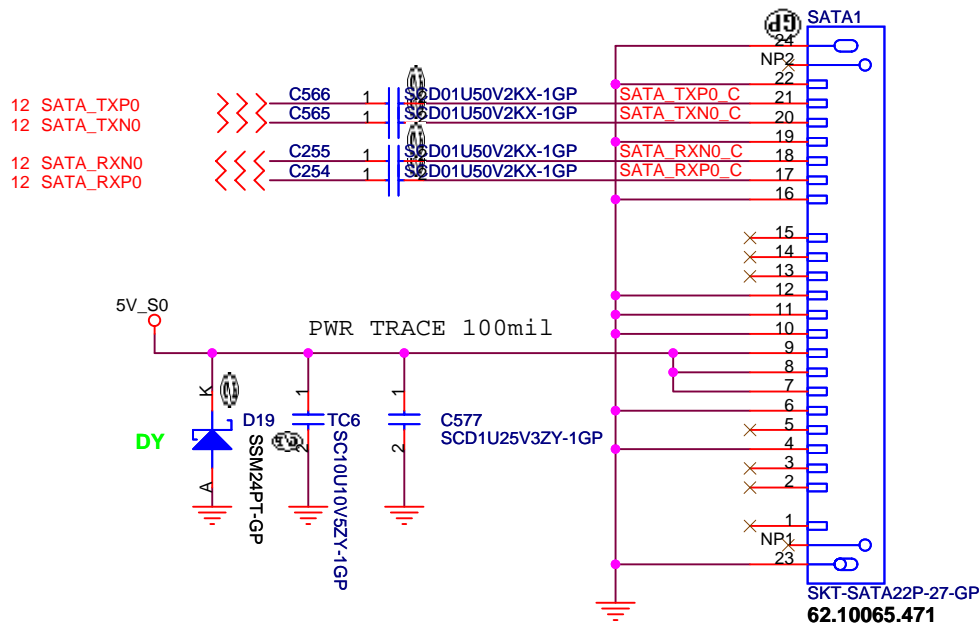
CRT CONN

JV50

SB



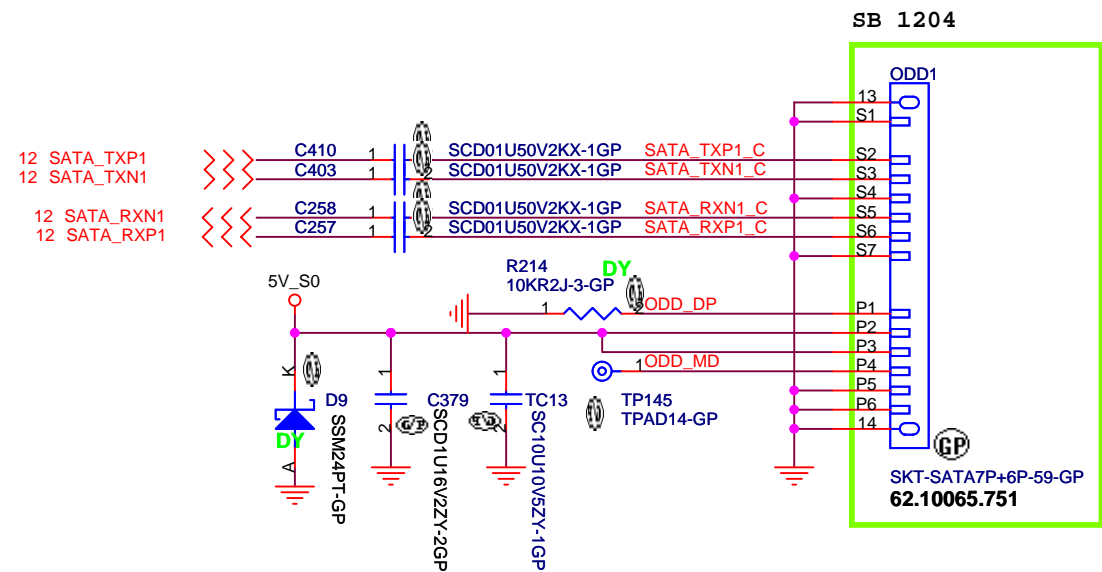
SATA Connector



JV50

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Title			
HDD CONN			
Size	Document Number		Rev
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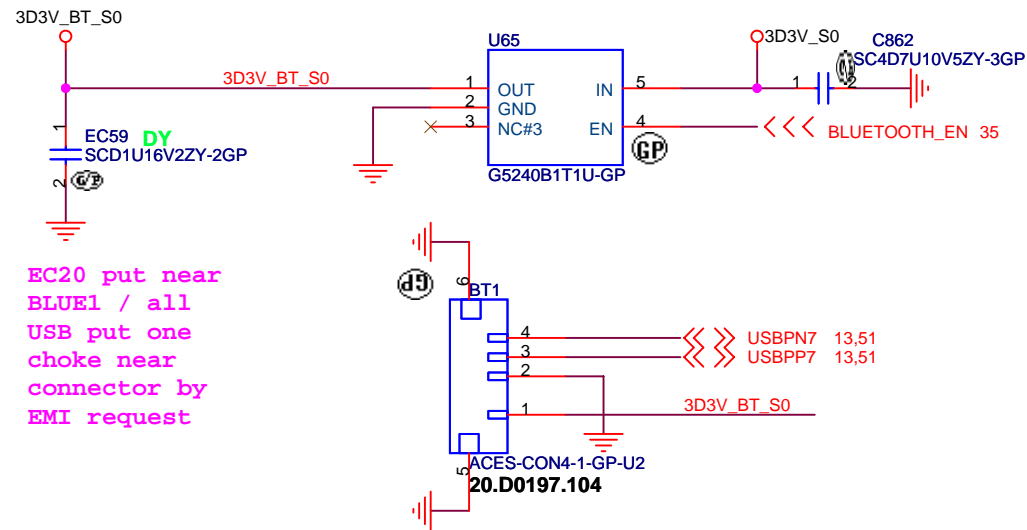
ODD Connector



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Title			
ODD			
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BLUETOOTH MODULE



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Title

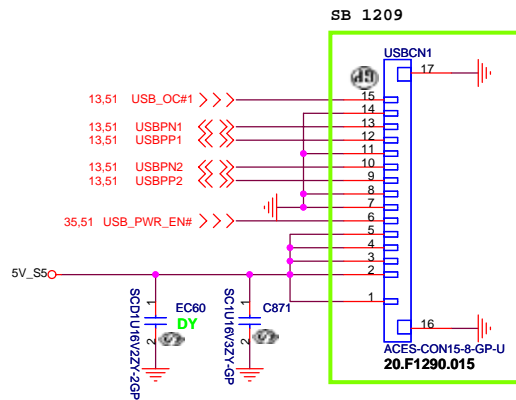
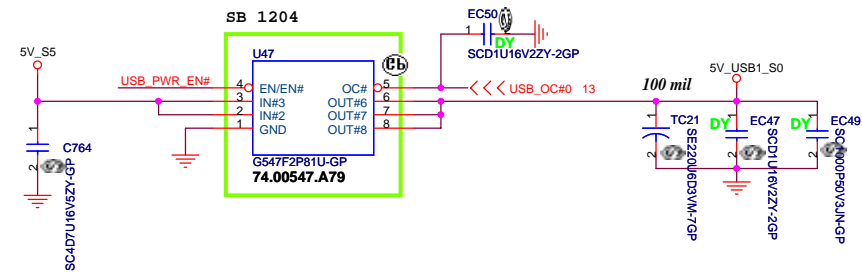
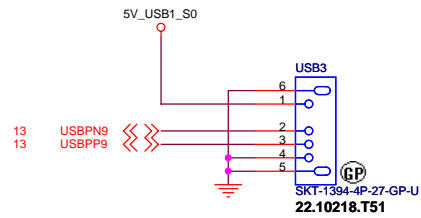
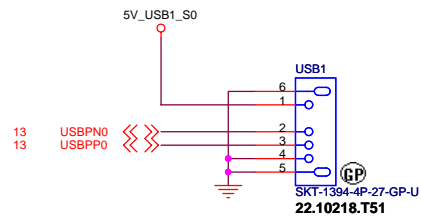
BLUETOOTH

Size Document Number Rev

JV50

SB

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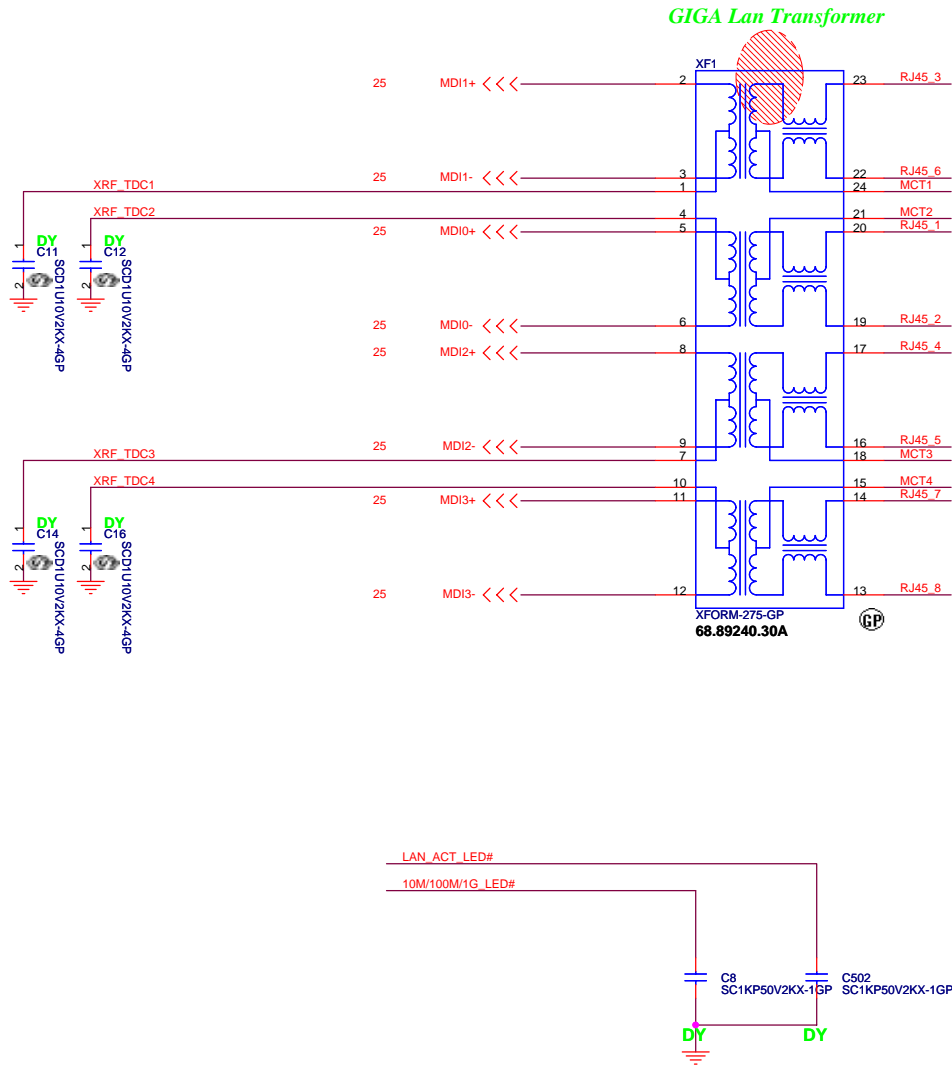


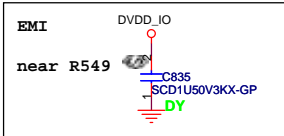
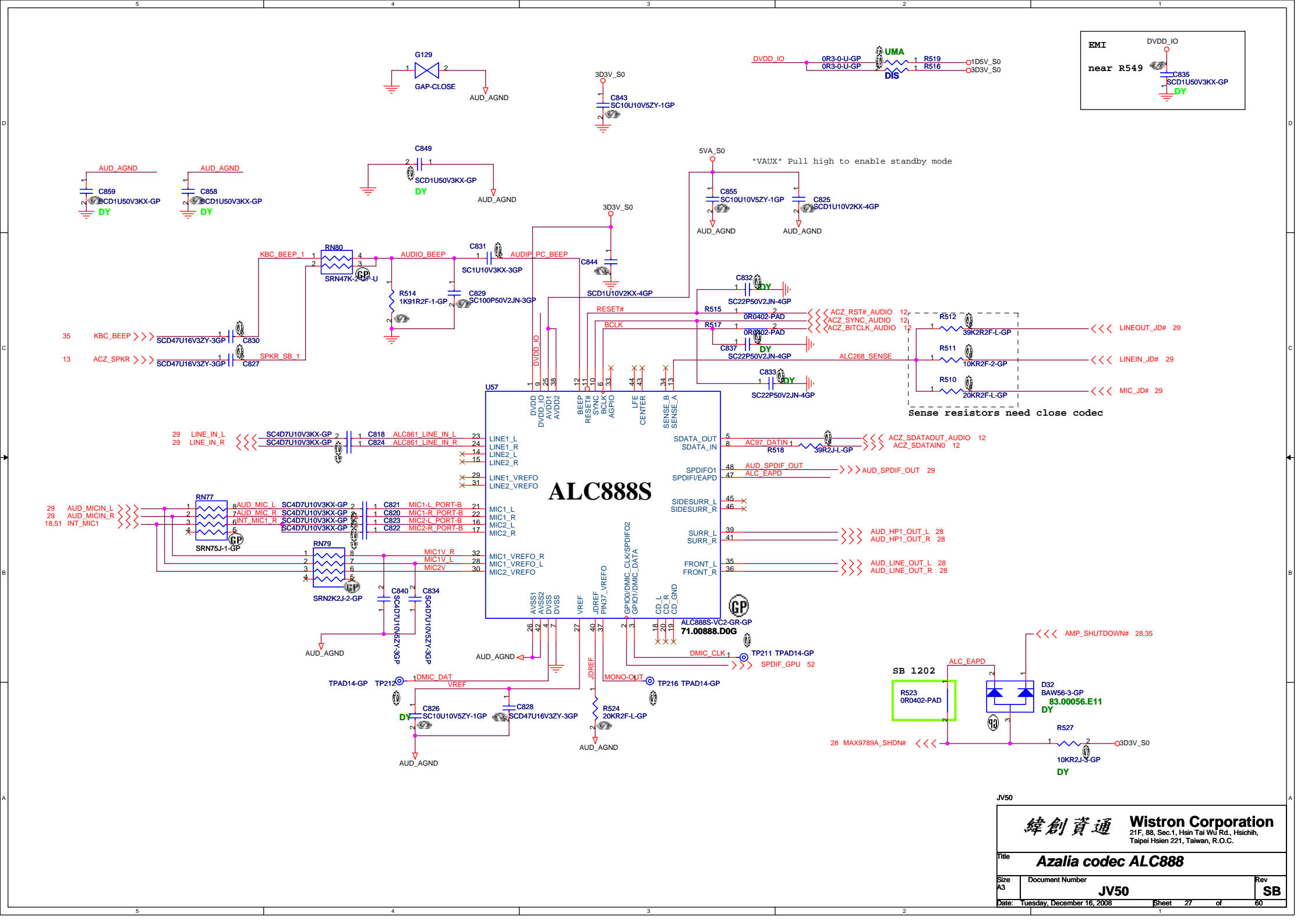
JV50

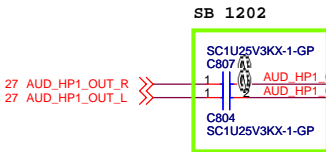
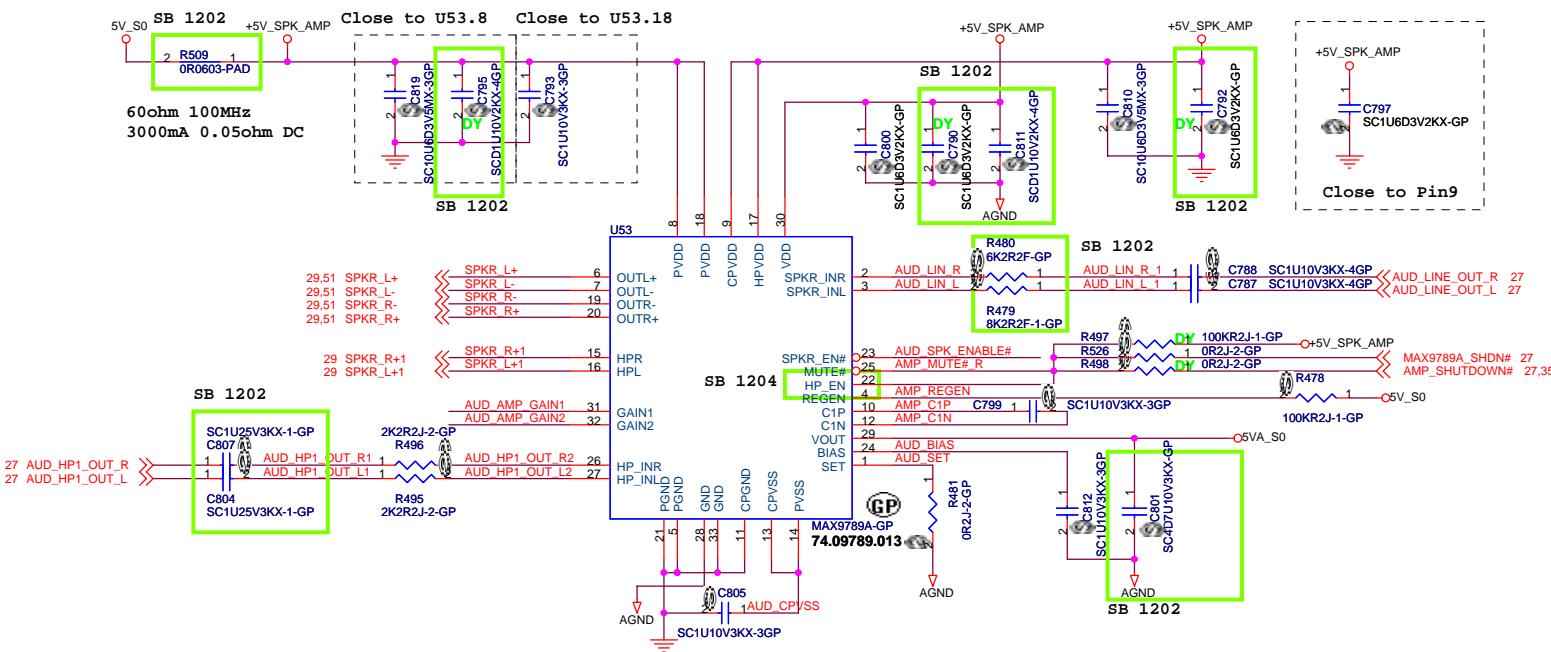
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
USB CONN			
Size	Document Number	Rev	SB
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector



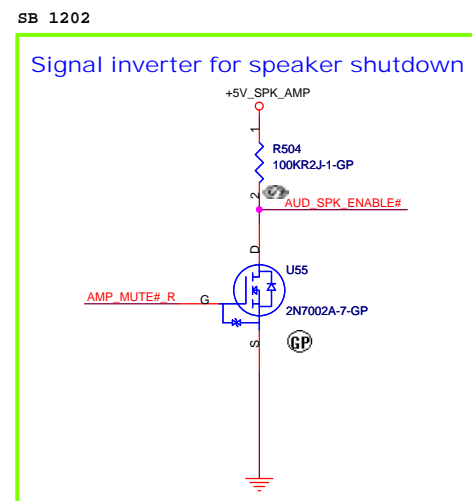
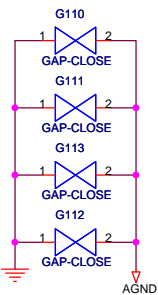




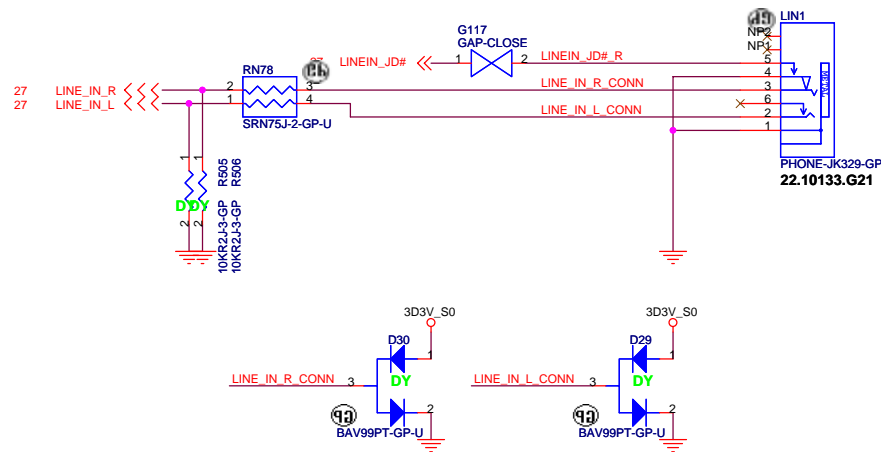
SB 1202

GAIN SETTING

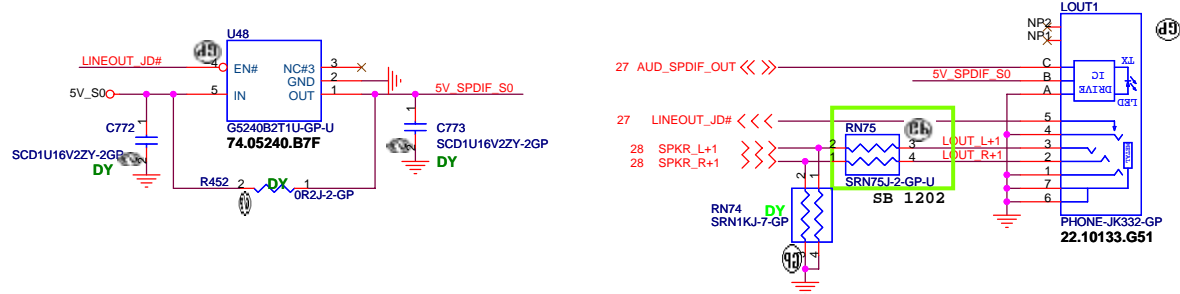
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



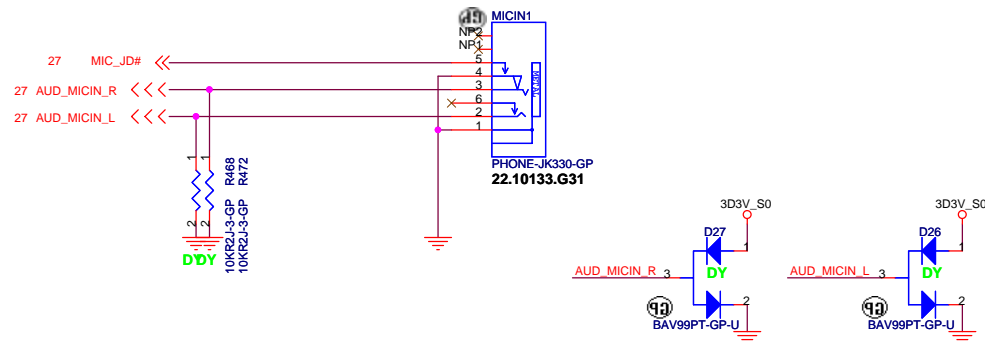
LINE IN



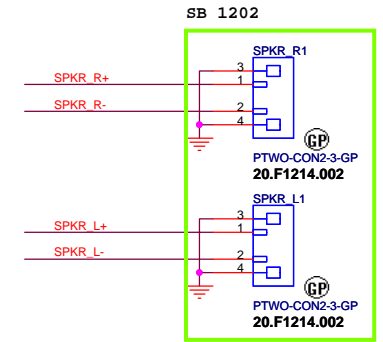
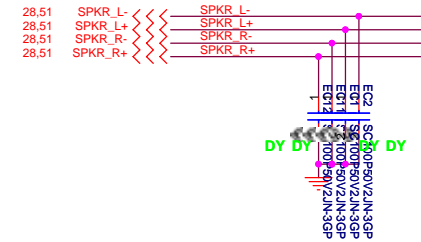
LINE OUT



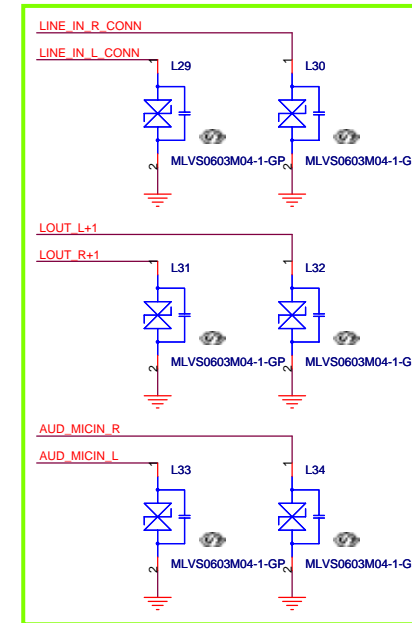
MIC IN



Internal Speaker

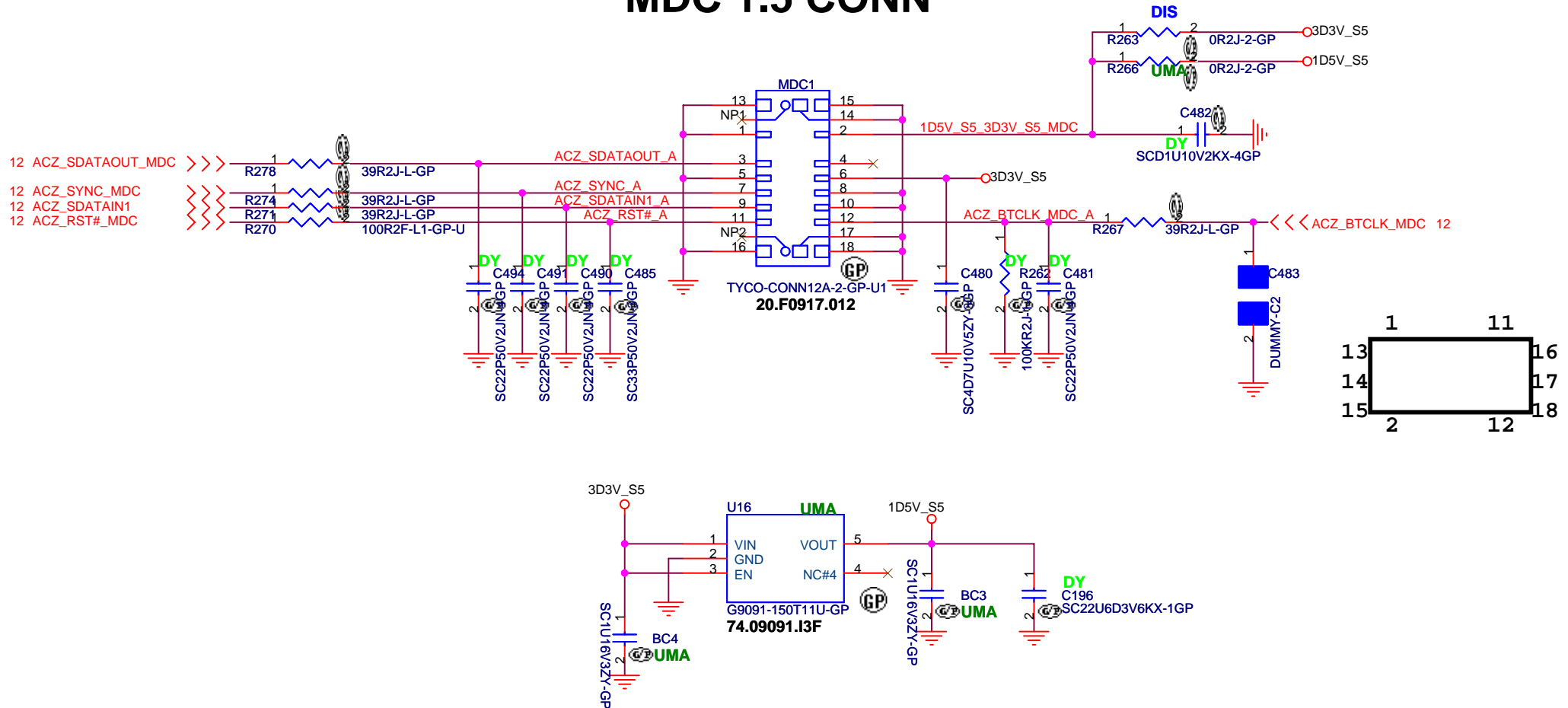


SB 1202



JV50

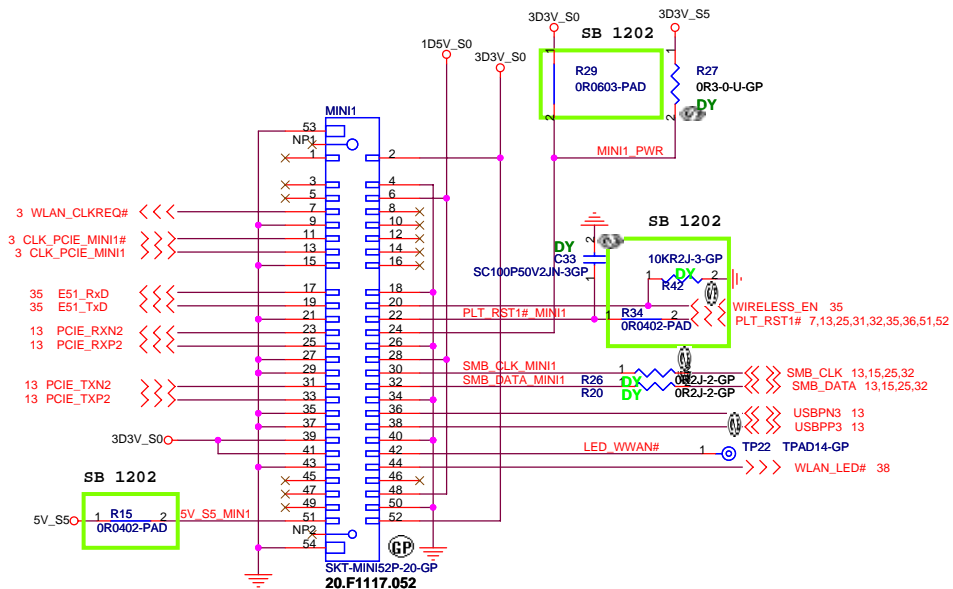
MDC 1.5 CONN



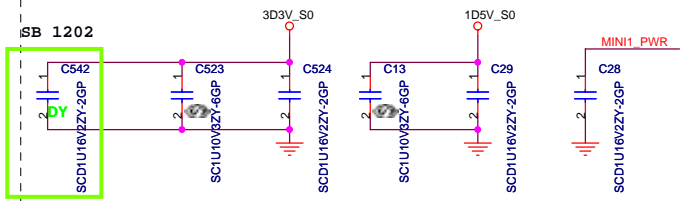
JV50

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Title			
MDC			
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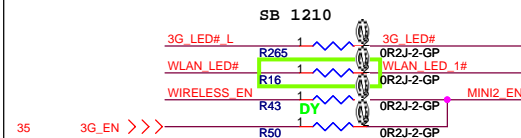
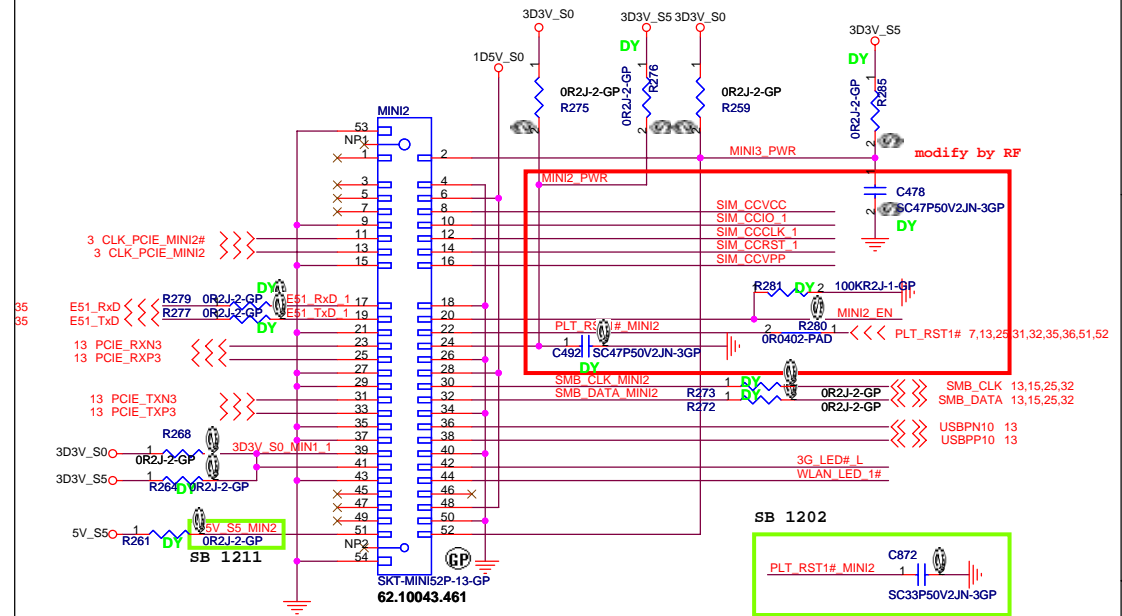
Mini Card Connector(WLAN) Support debug-card



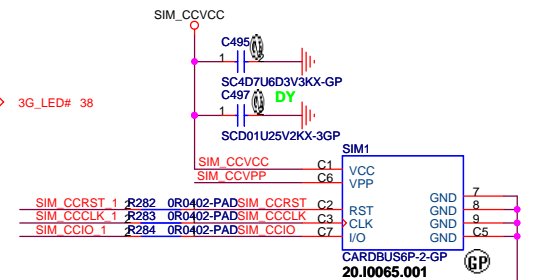
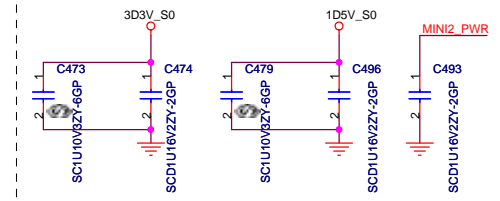
Place near MINI1



Mini Card Connector(Robson2 and 3G)



Place near MINIC2



JV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARDSize
A3

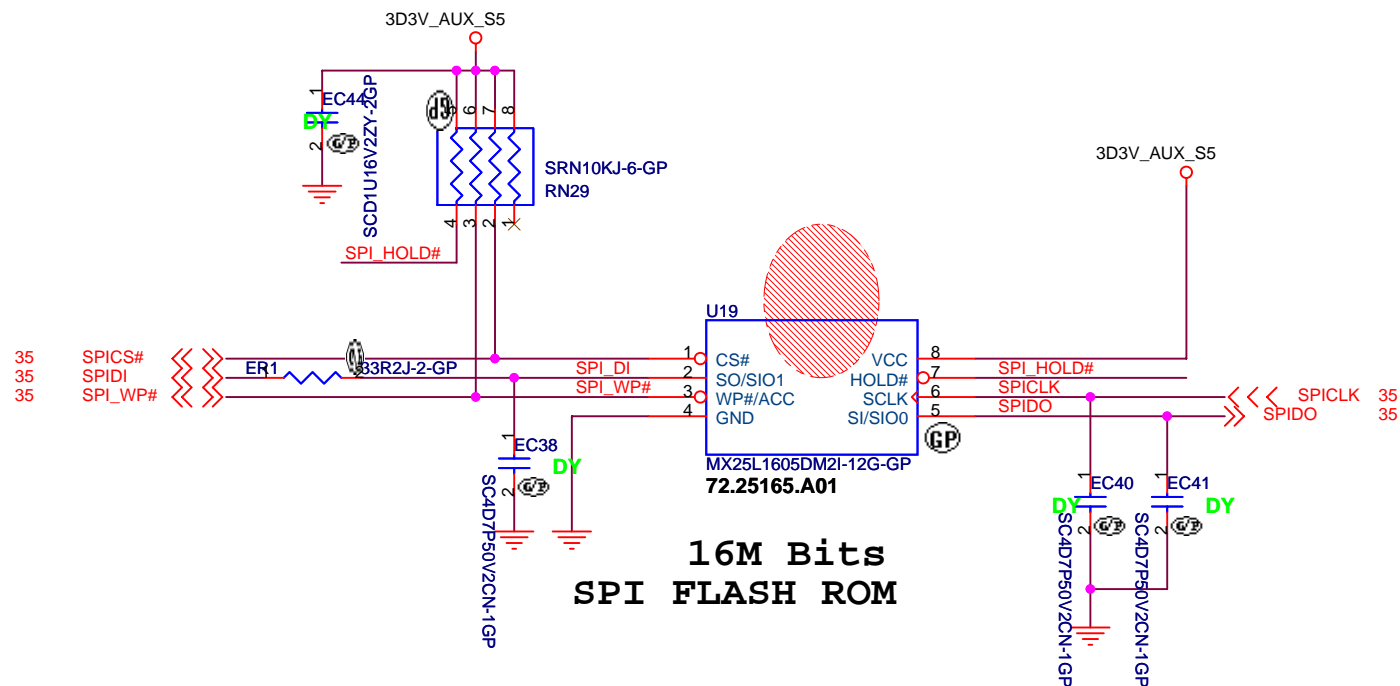
Document Number	
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JV50

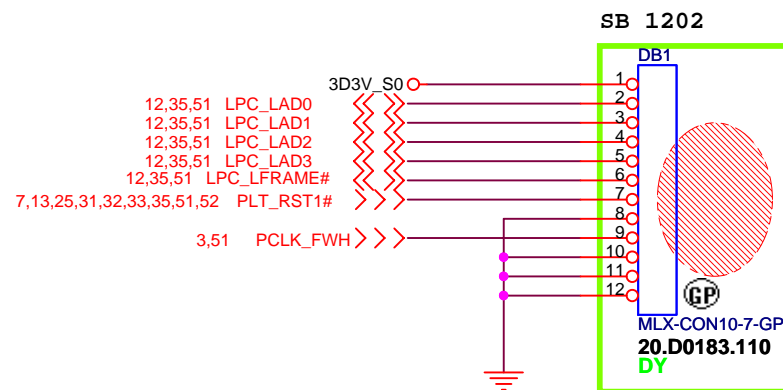
Date: Tuesday, December 16, 2008

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Rev
SR



GOLDEN FINGER FOR DEBUG BOARD



JV50

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Title

BIOS

Size

Document Number

Rev

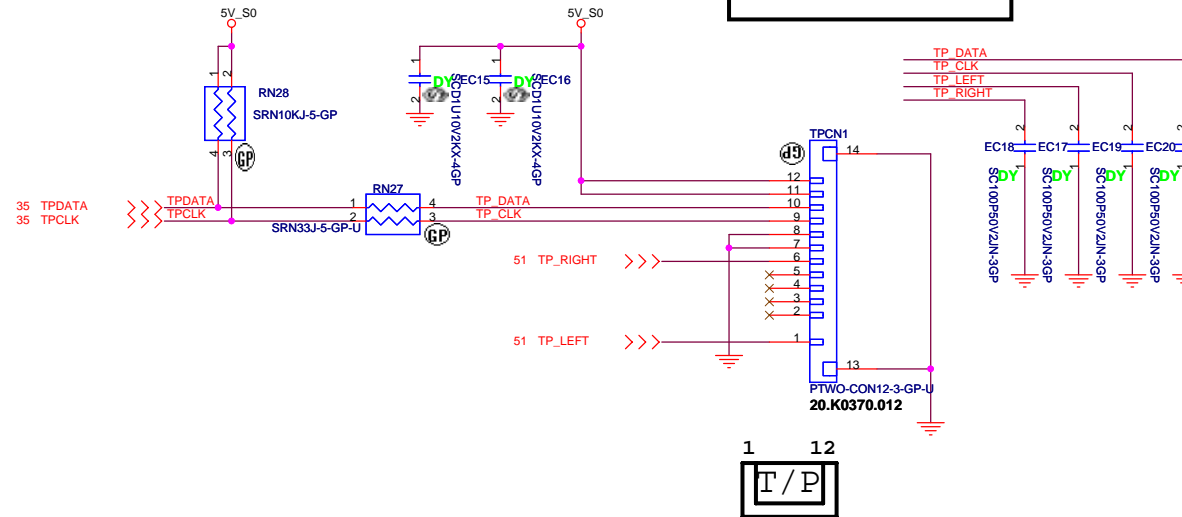
JV50

SB

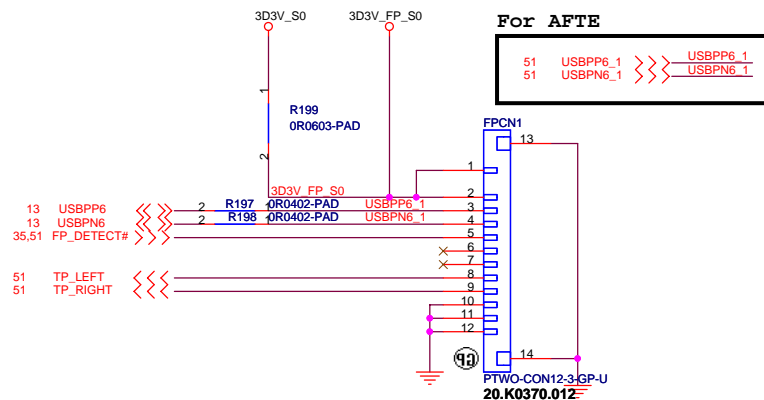
Date: Tuesday, December 16, 2008

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TOUCH PAD



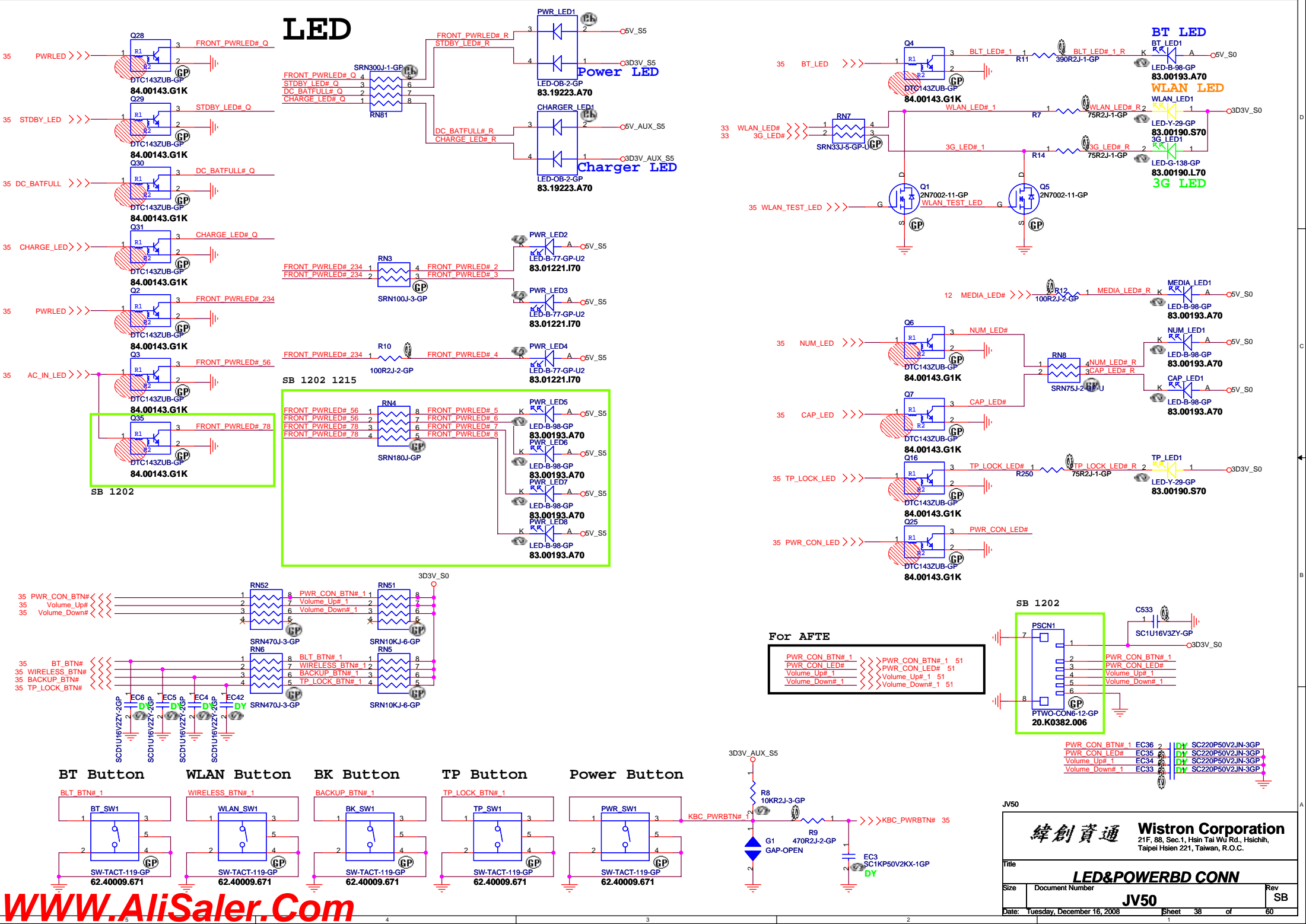
Finger printer

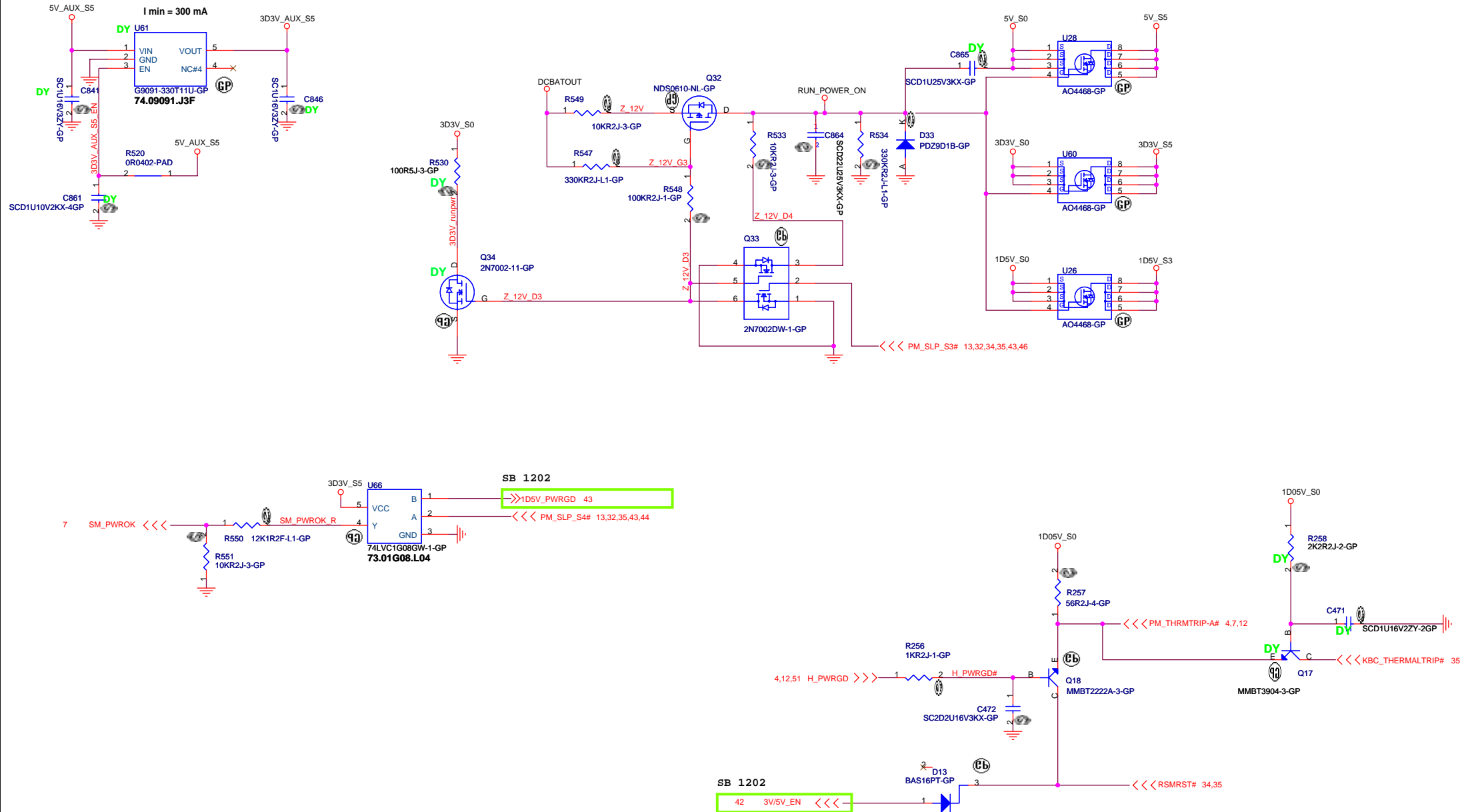


JV50

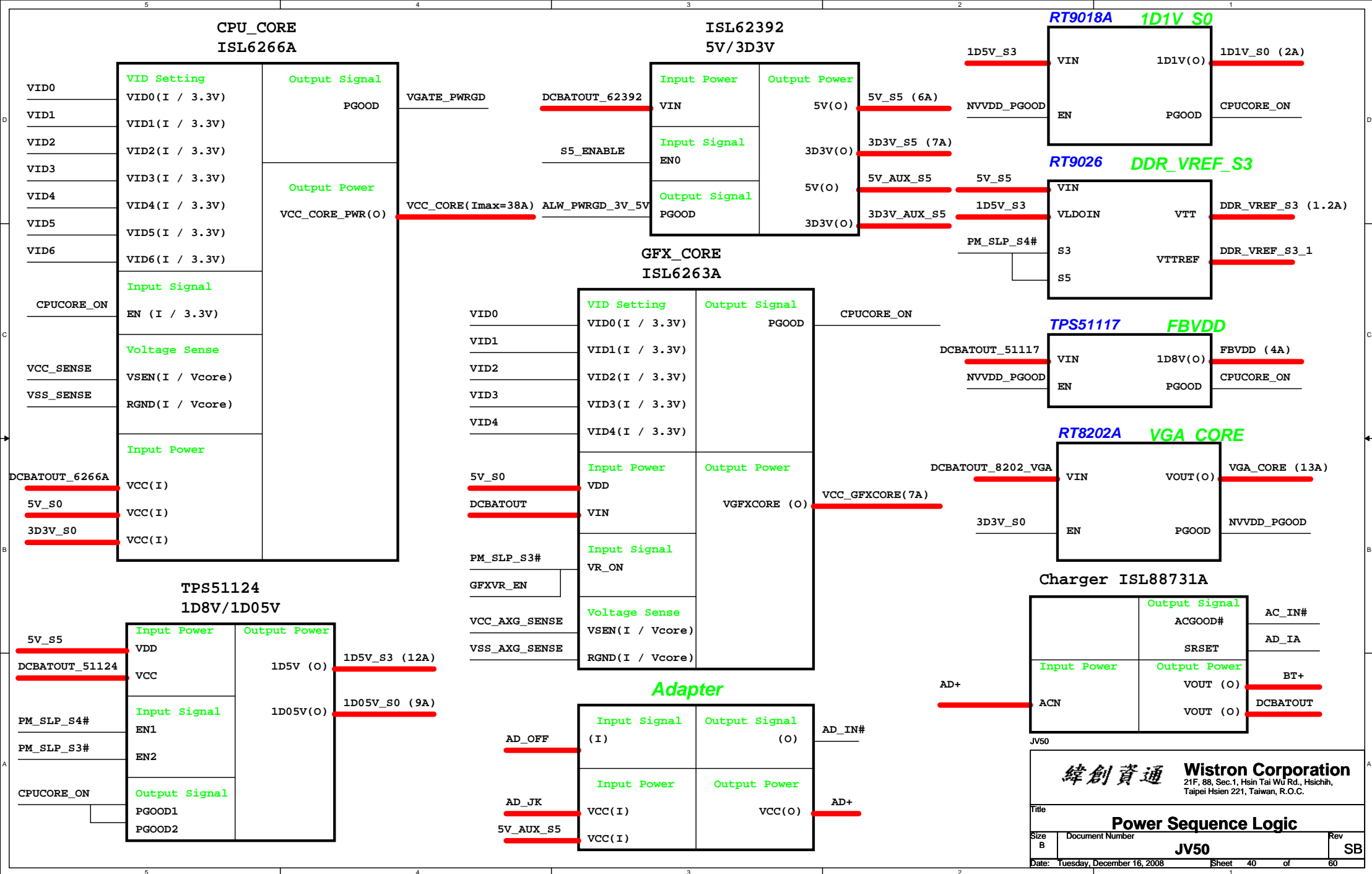
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Touch PAD and FP			
Size Document Number	Rev SB		
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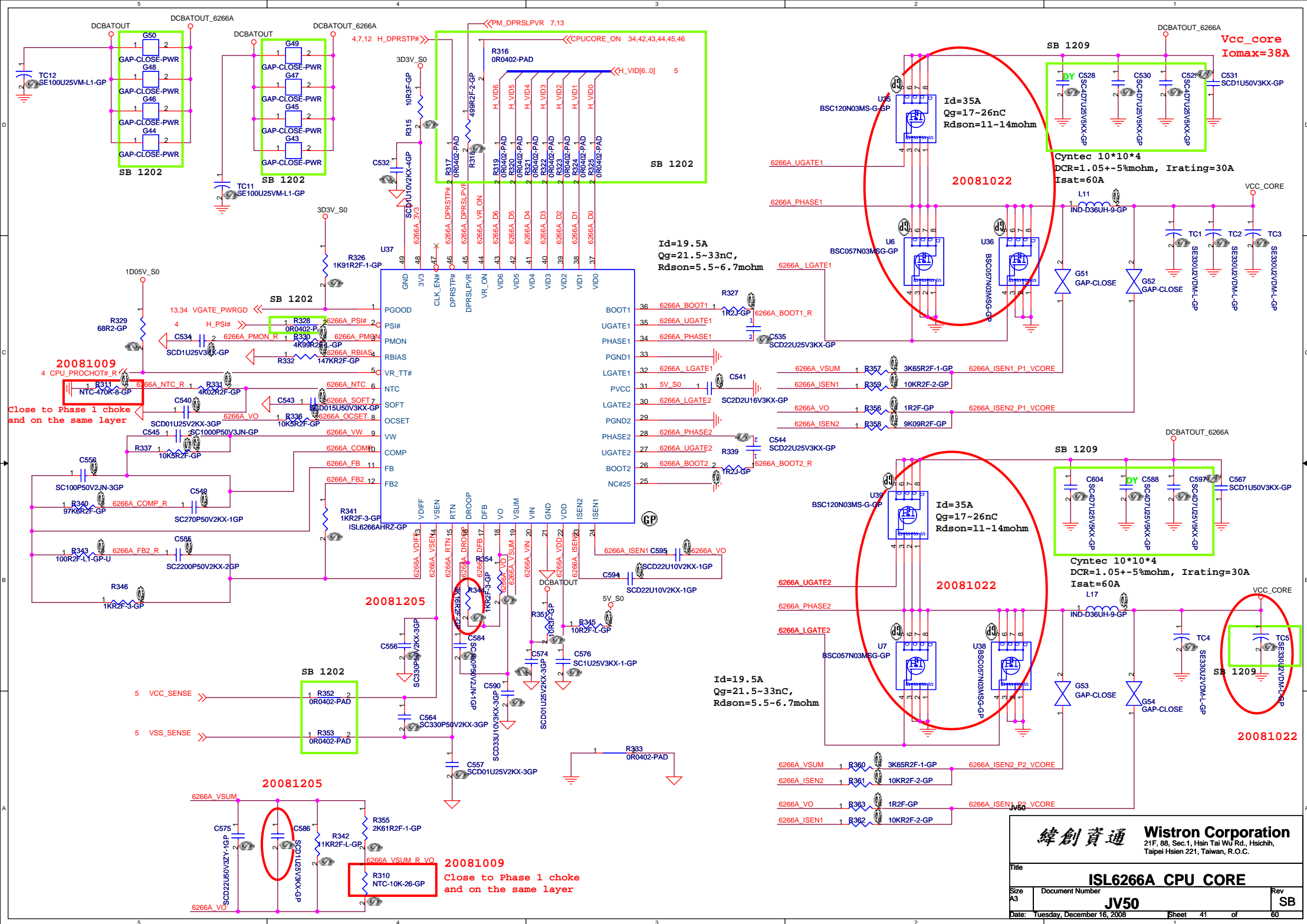
LED

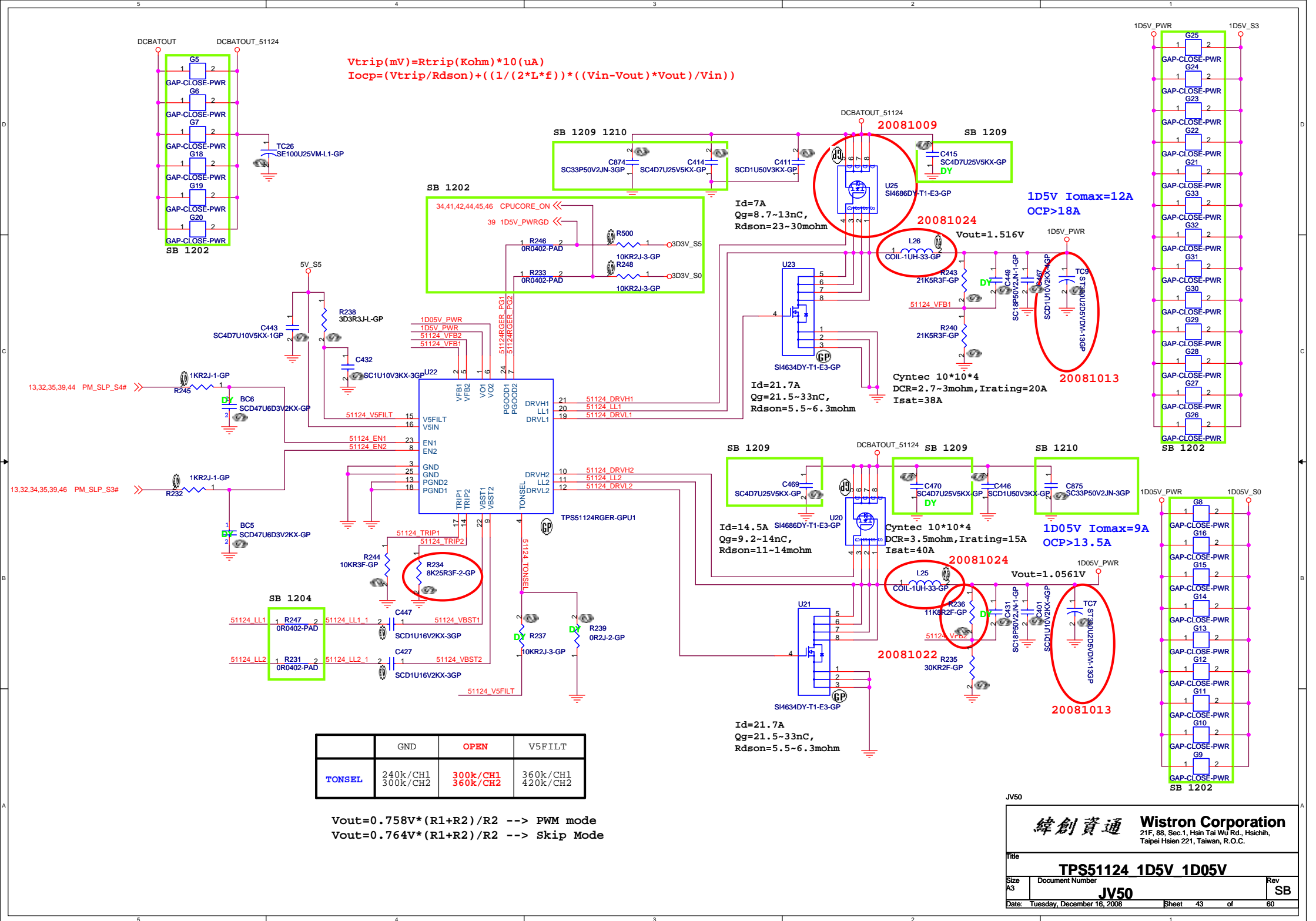


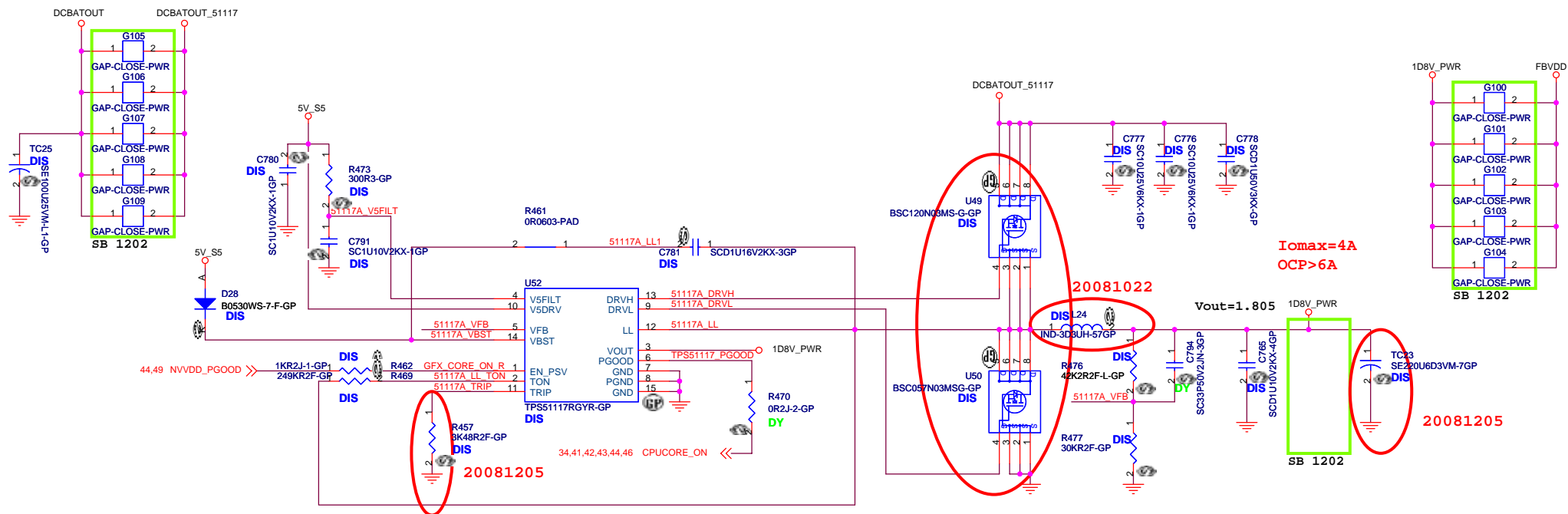


JV50









$$V_{out} = 0.75V * (R1 + R2) / R2$$

JV50

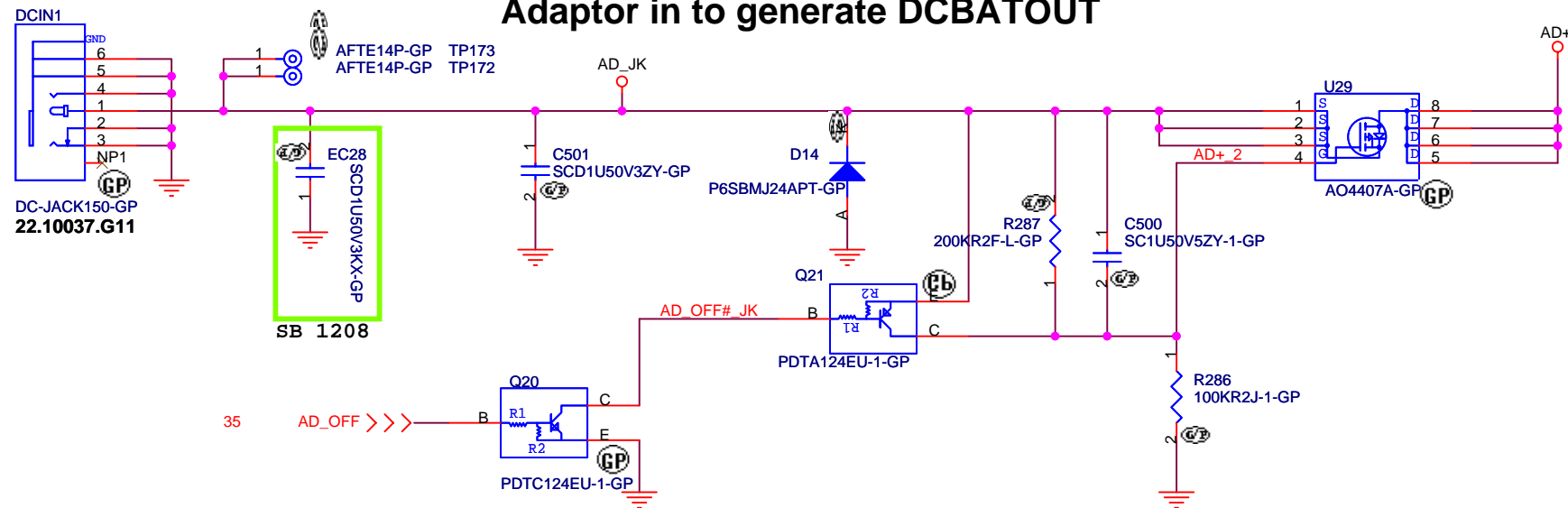
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS51117 1D8V		
Size	Document Number	Rev
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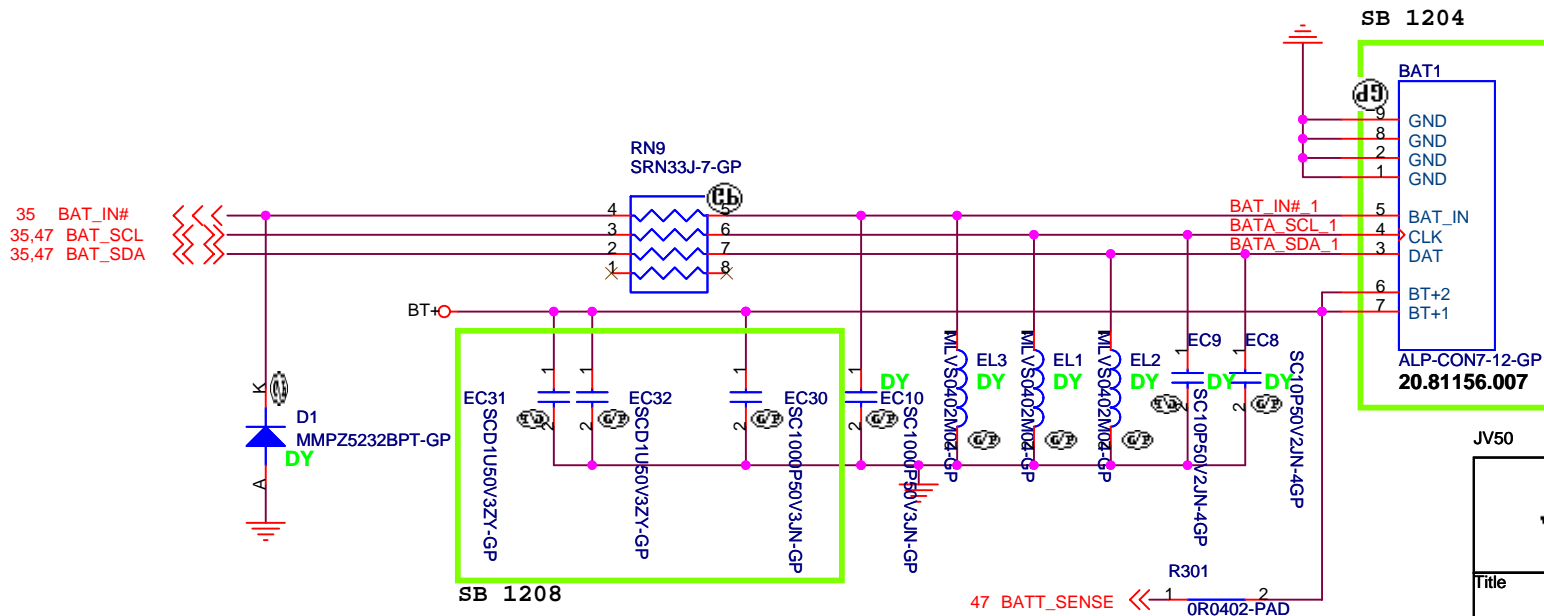


Title			
ISL88731A Charger			
Size A3	Document Number		Rev
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Adaptor in to generate DCBATOUT



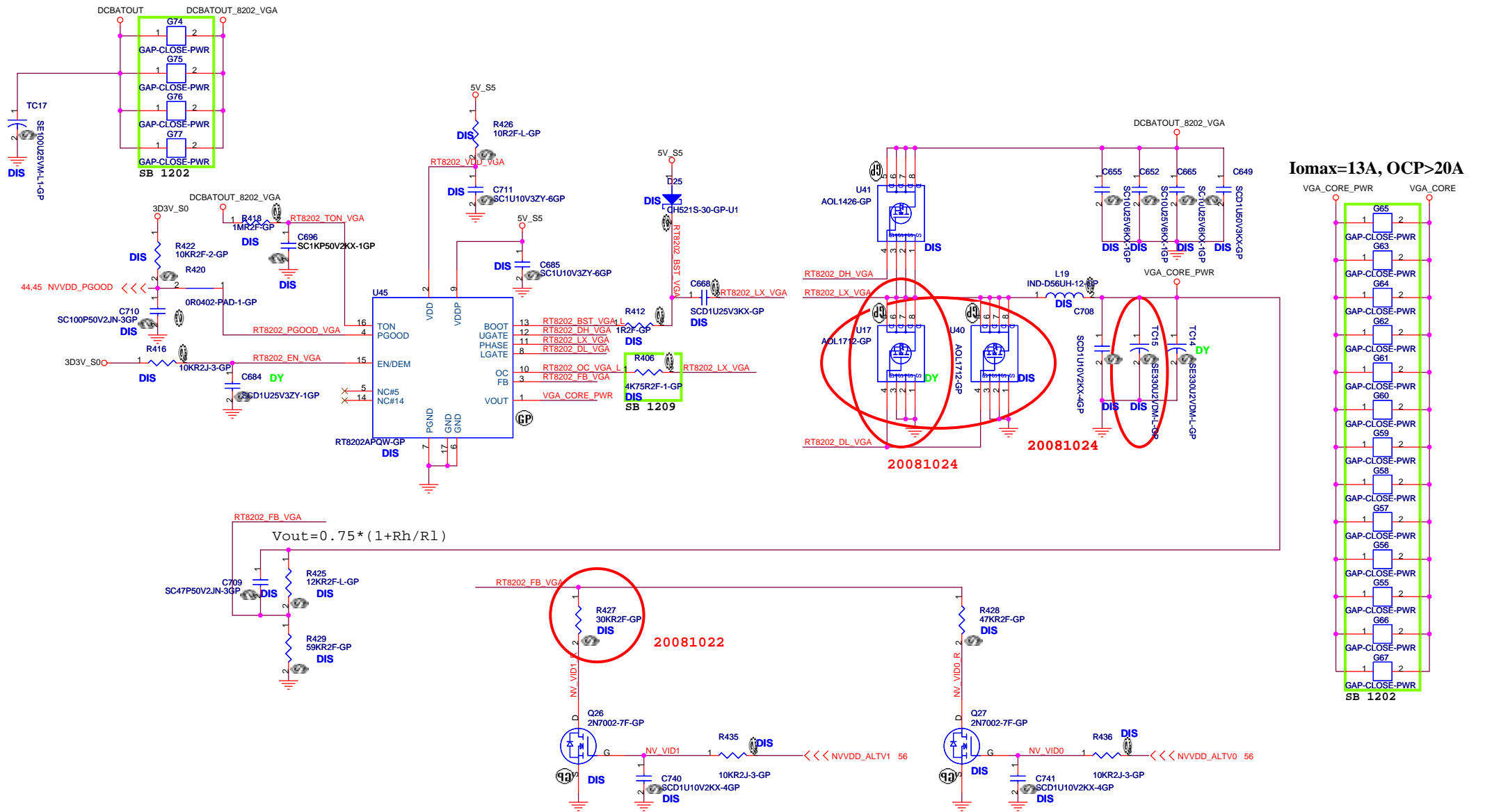
BATTERY CONNECTOR



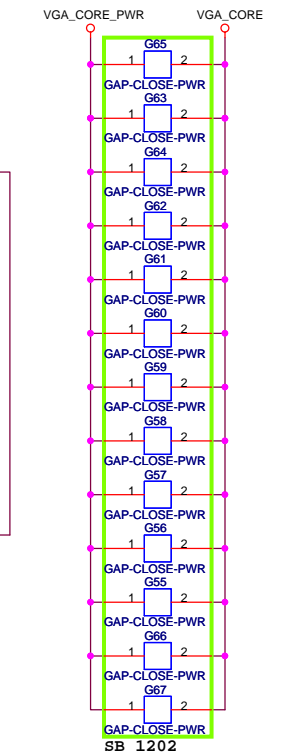
緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
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Iomax=13A, OCP>20A

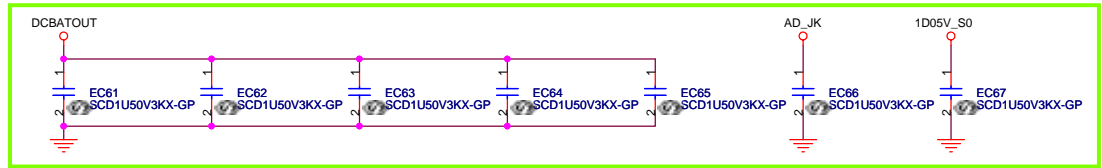


$$V_{out} = 0.75 * (1 + R_h / R_l)$$

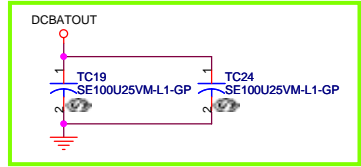
N10M-GE1		
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

JV50

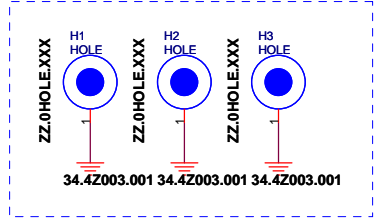
SB 1208



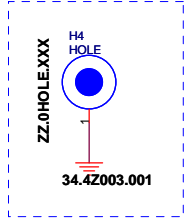
SB 1209



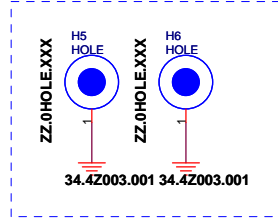
CPU



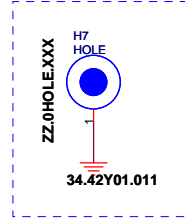
NB



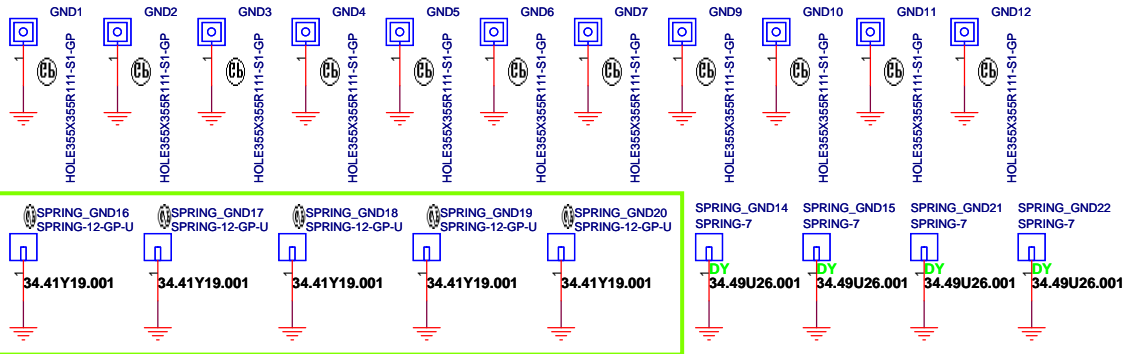
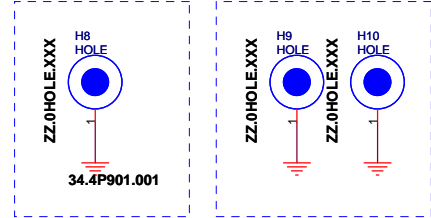
VGA



MDC



MINICARD



JV50

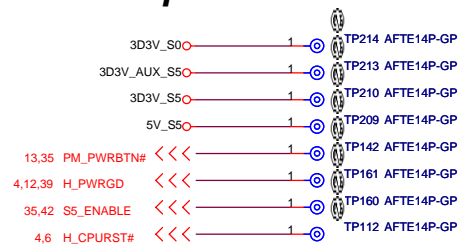
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Taipei Hsien 221, Taiwan, R.O.C.

Title EMI/Spring/Boss

Size Document Number Rev SB

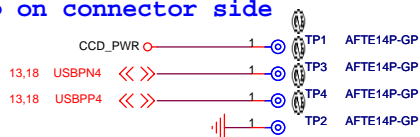
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Check test point

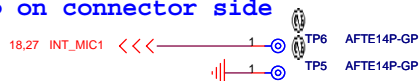


Test Point放在Dimm Door打開可量測處

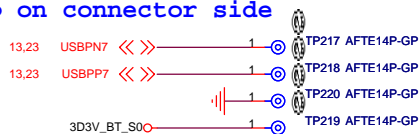
CCD1 Conn. Test Point keep on connector side



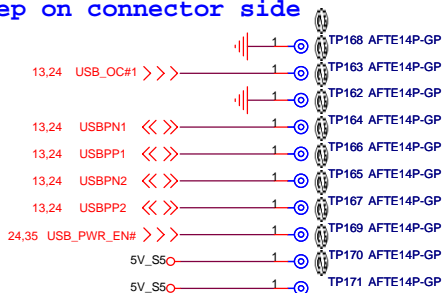
AMIC1 Conn. Test Point keep on connector side



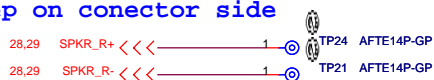
BT1 Conn. Test Point keep on connector side



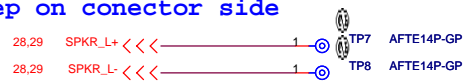
USBCN1 Conn. Test Point keep on connector side



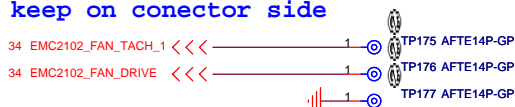
SPKR_R1 Conn. Test Point keep on connector side



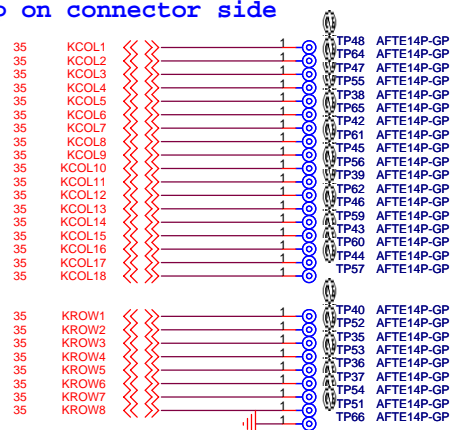
SPKR_L1 Conn. Test Point keep on connector side



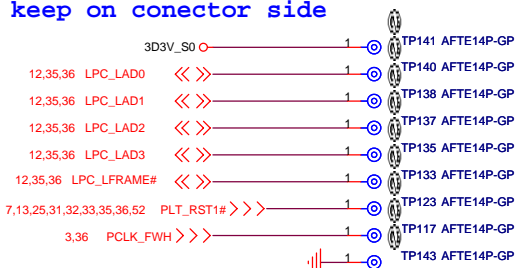
FAN1 Conn. Test Point keep on connector side



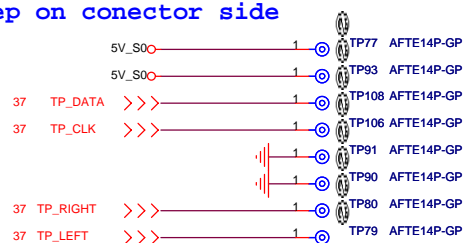
KB1 Conn. Test Point keep on connector side



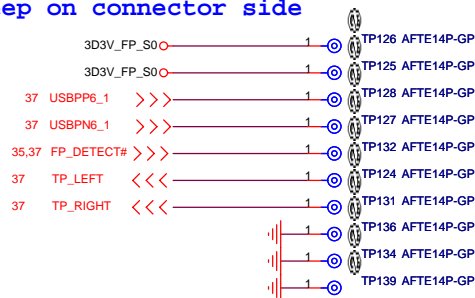
DB1 Conn. Test Point keep on connector side



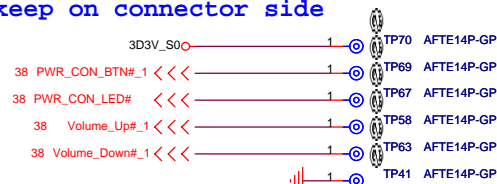
TPCN1 Conn. Test Point keep on connector side



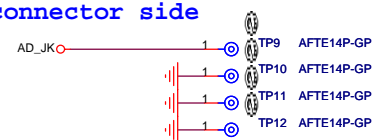
FPCN1 Conn. Test Point keep on connector side



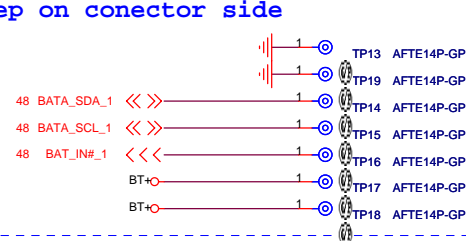
PSCN1 Conn. Test Point keep on connector side



DCIN1 Conn. Test Point keep on connector side



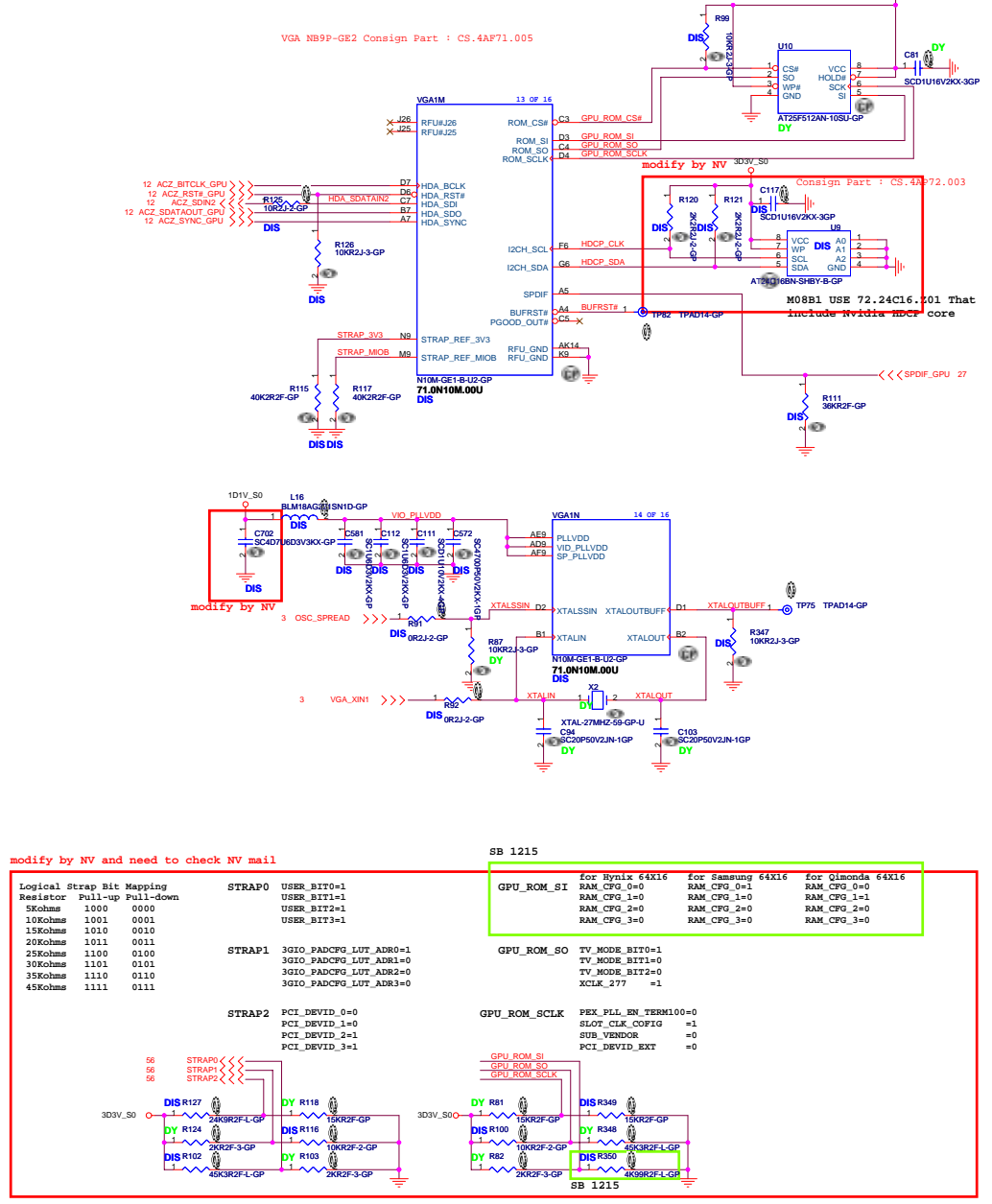
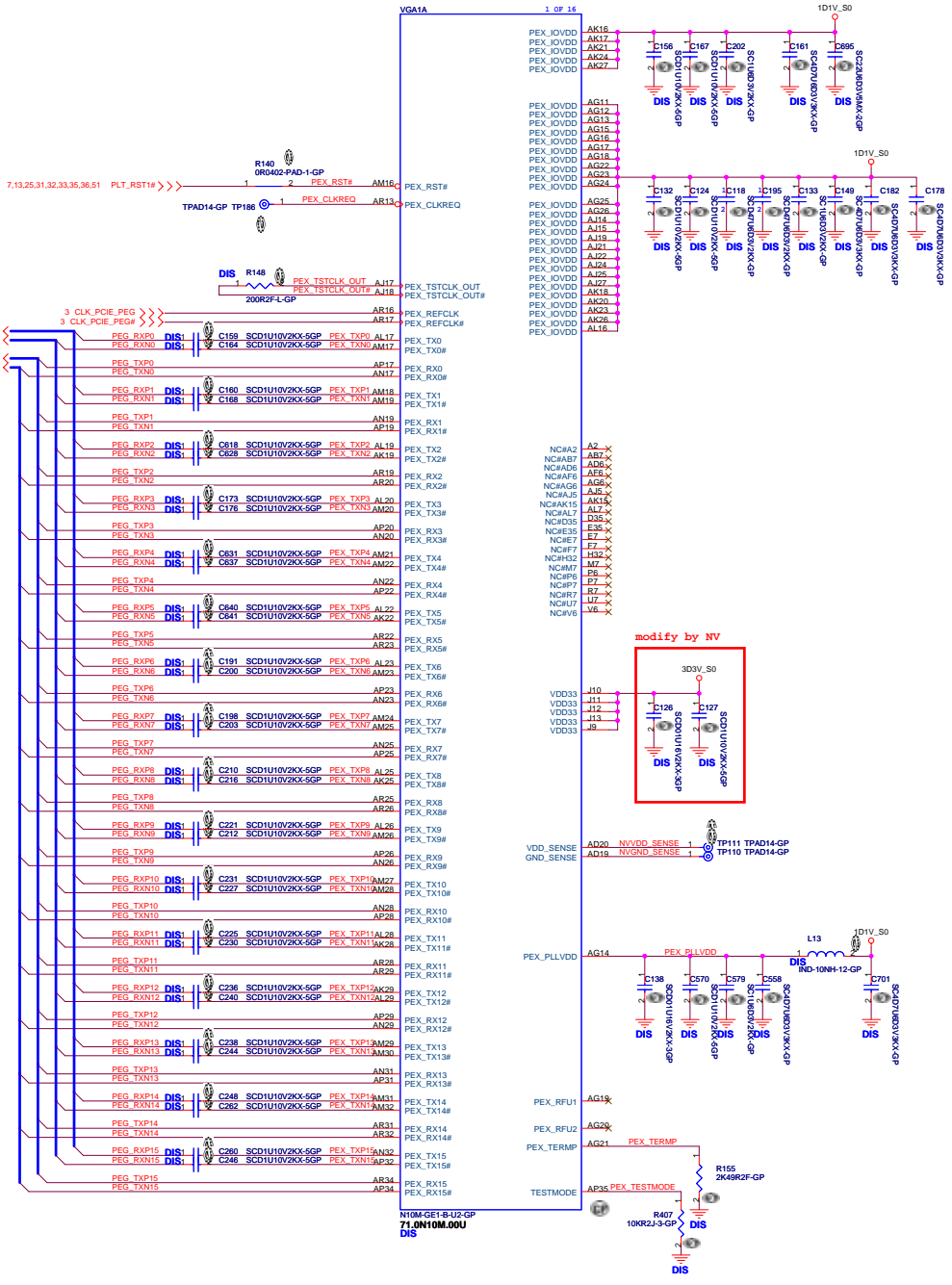
TPCN1 Conn. Test Point keep on connector side



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modify by NV and need to check NV mail

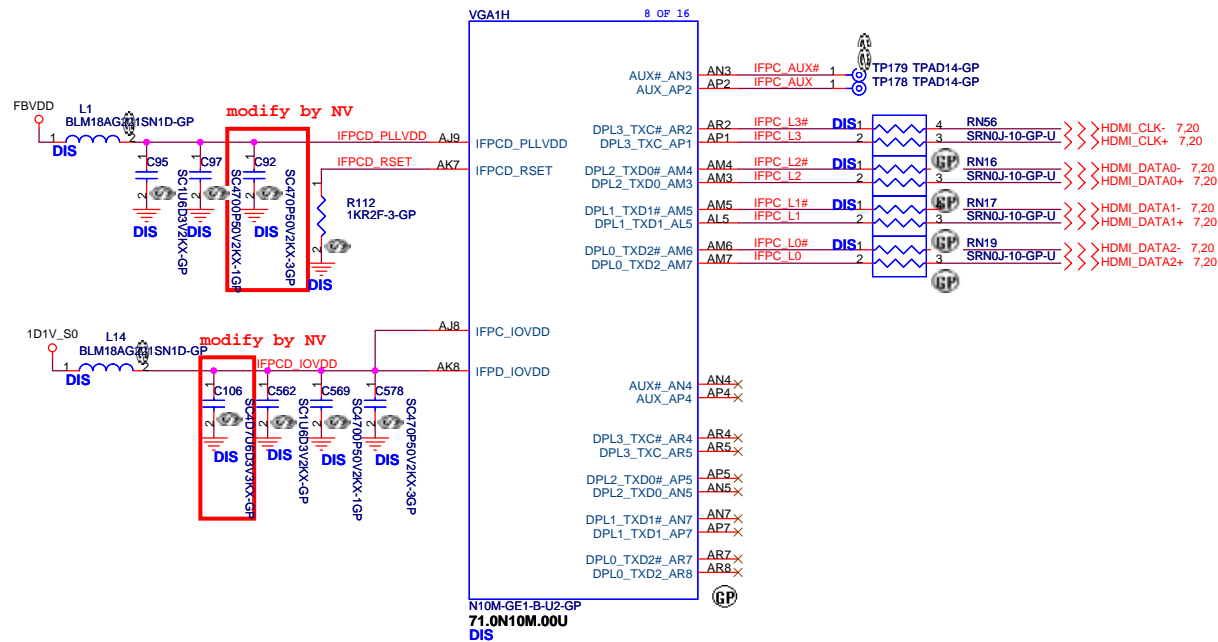
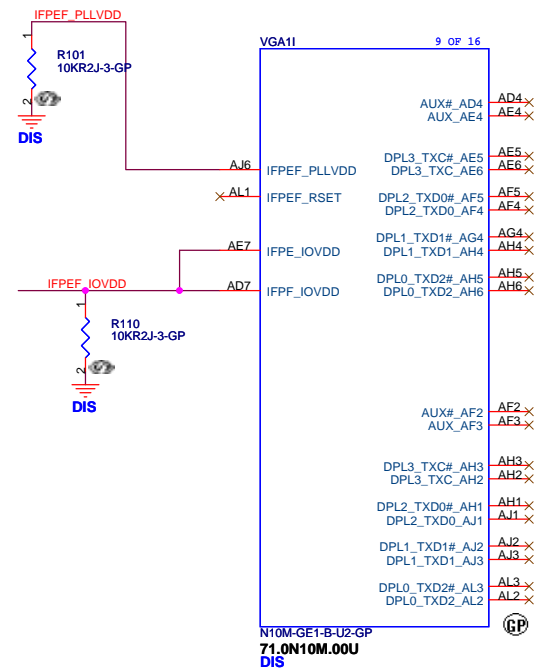
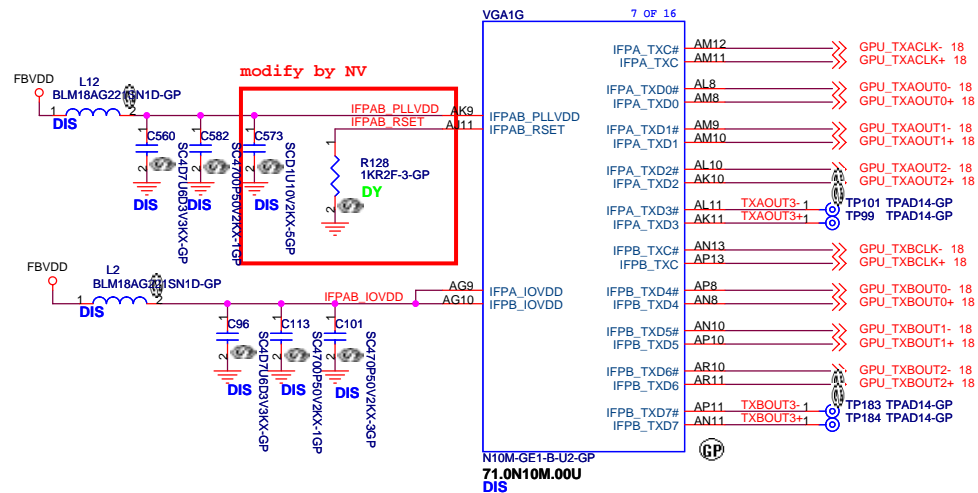
Logical Strap Bit Mapping	Resistor	Strap0	Strap1	Strap2
Pull-up	50kOhms	1000	0000	
Pull-down	10kOhms	1001	0001	
	15kOhms	1010	0010	
	20kOhms	1011	0011	
	25kOhms	1100	0100	
	30kOhms	1101	0101	
	35kOhms	1110	0110	
	45kOhms	1111	0111	

SB 1215

GPU_ROM_SI	GPU_ROM_SO	GPU_ROM_SCLK
for Hynix 64X16	for Samsung 64X16	for Qimonda 64X16
RAM_CFG_0=0	RAM_CFG_0=1	RAM_CFG_0=0
RAM_CFG_1=0	RAM_CFG_1=1	RAM_CFG_1=1
RAM_CFG_2=0	RAM_CFG_2=1	RAM_CFG_2=0
RAM_CFG_3=0	RAM_CFG_3=1	RAM_CFG_3=0

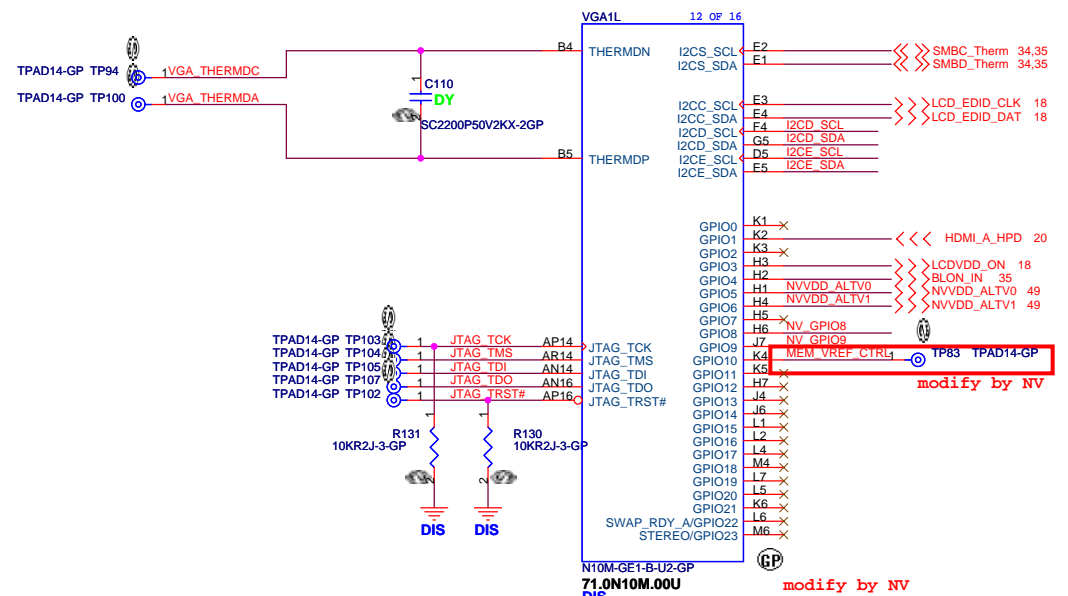
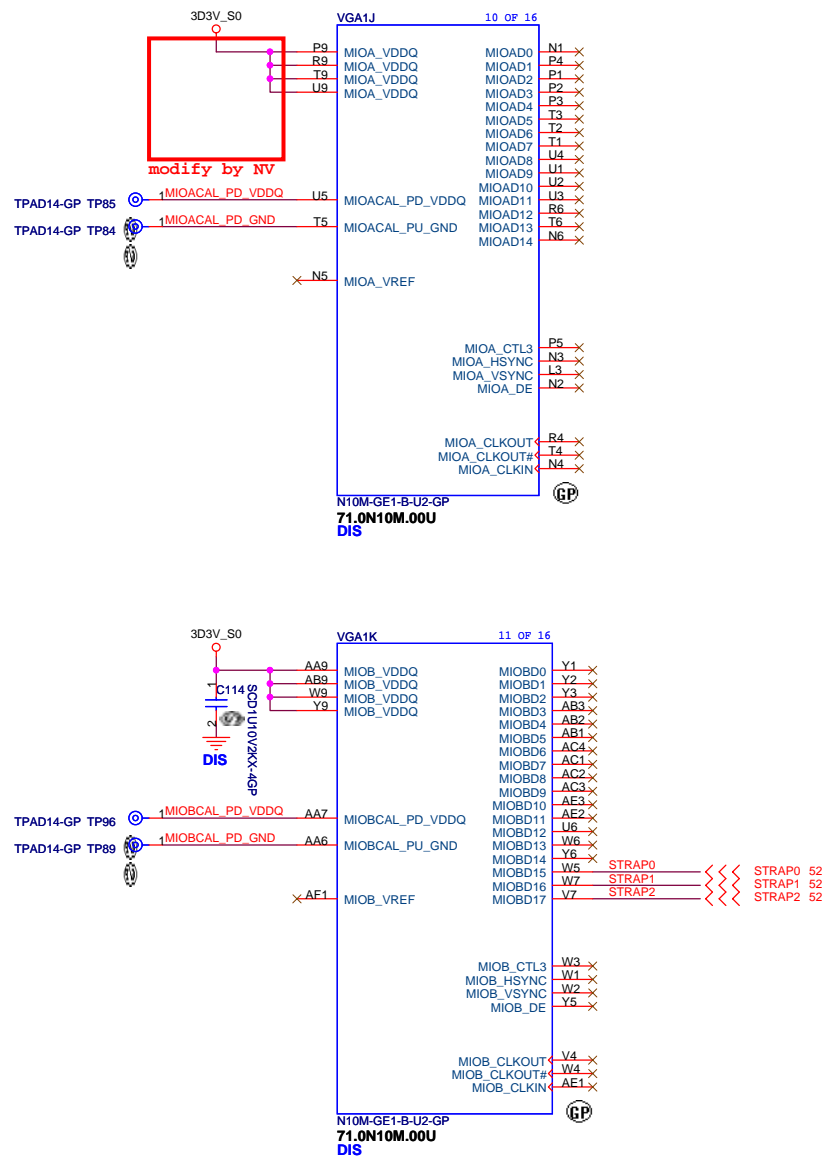
GPU_ROM_SI TV_MODE_BIT0=1
GPU_ROM_SO TV_MODE_BIT1=0
GPU_ROM_SCLK TV_MODE_BIT2=0
XCLK_277 =1

GPU_ROM_SCLK PEK_PLL_BN_TERM100=1
SLOT_CLK_CFG1 =1
SUB_VENDOR =0
PCI_DEVID_EXT =0



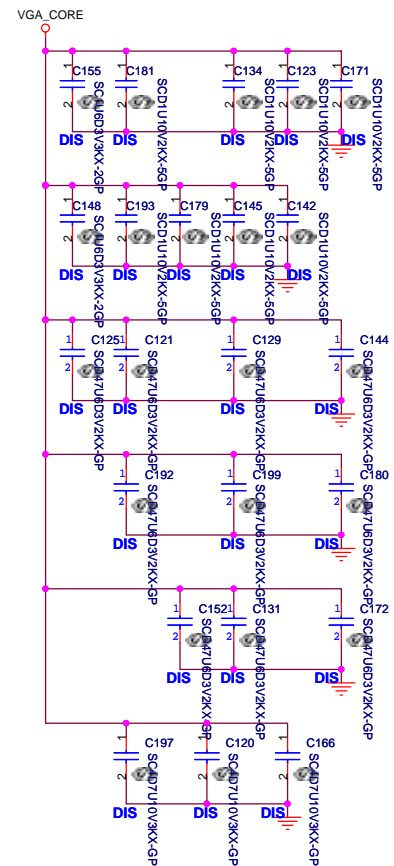
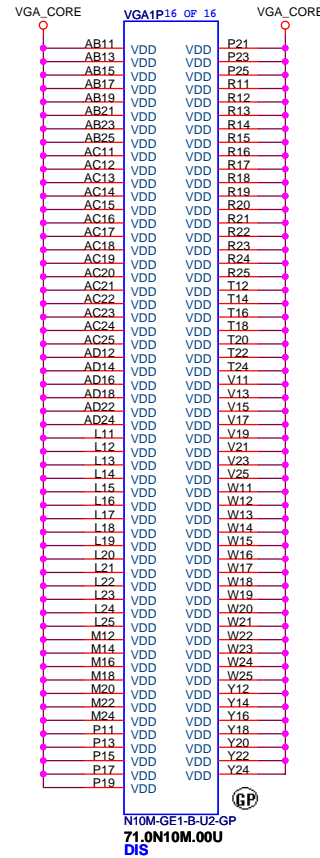
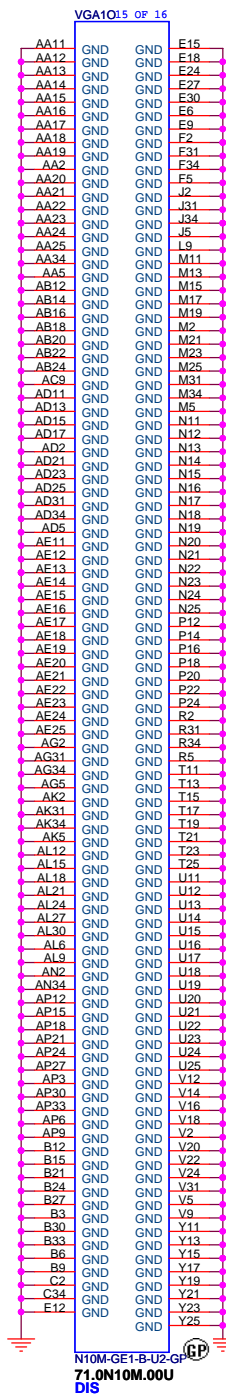
JV50

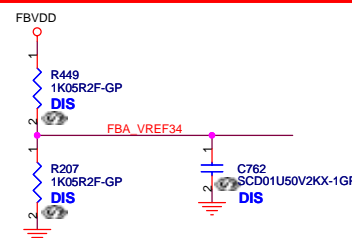
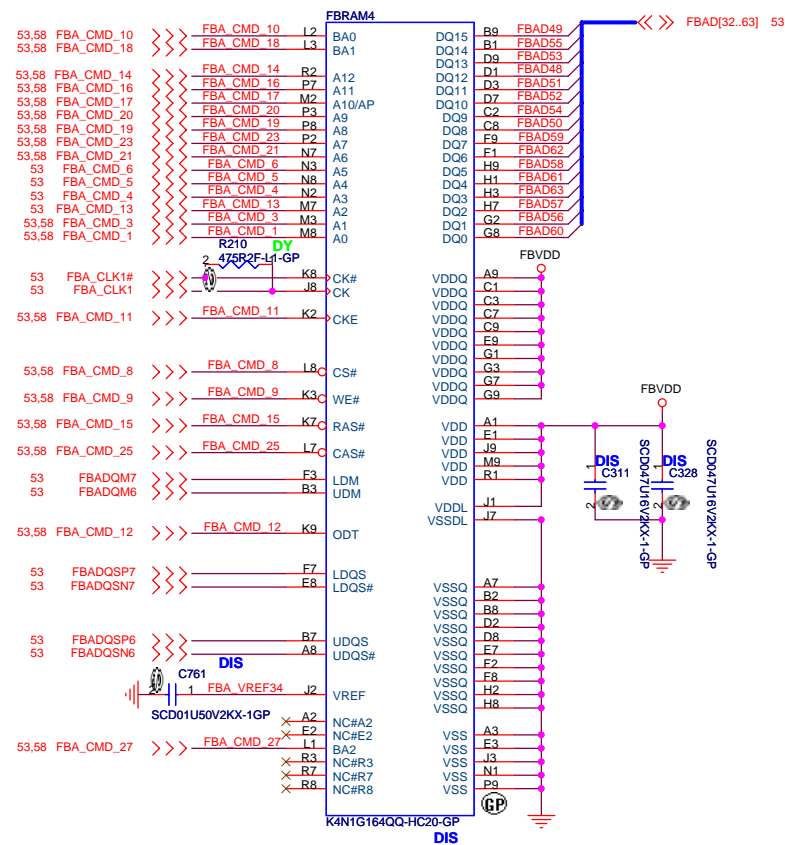
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SB
All Component for NB9P-GE2

Page3: change C452 C453 from 27P to 33P by vendor's request

Page33: add C872 33P for SIV

Page29: change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page18: change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request

Page24: change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request

Page38: change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request

Page18: change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request

Page3: add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0

Page3: change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount

Page7: change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection

Page9: change C275 from UMA to DY and change C349 from mount to DY

Page10: change C243 C758 from mount to DY and change R167 R398 from DIS to DY

Page13: change R216 from 0ohm resistor to 0ohm pad

Page14: change C413 C252 C703 C392 C707 C734 from mount to DY

Page17: change C426 C429 from mount to DY

Page18: change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA

Page20: add RN86 for DIS HDMI SMBus

Page25: change R45 from 0ohm resistor to 0ohm pad

Page27: change R523 from 0ohm resistor to 0ohm pad

Page7: add R556 pull-low DY for A1 NB

Page28: change AGND & GND and change R509 from 0ohm resistor to 0ohm pad

Page28: change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2

Page28: combine C801 C802 two 1u to C801 4.7u

Page28: delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31

Page28: change R474 from DY to mount and change R475 from mount to DY for 10dB

Page29: add L29 L30 L31 L32 L33 L34 for ESD

Page31: change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad

Page32: change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad

Page12: change C385 C386 from 10p to 7p by vendor's request

Page35: change C136 C169 from 15p to 7p by vendor's request

Page33: change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY

Page34: change C42 from mount to DY

Page35: change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version

Page36: change DB1 from mount to DY

Page38: add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type

Page39: change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN

Page40: update power sequence logic

Page41: change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad

Page42: change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap

Page43: change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap

Page43: change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5

Page45: change G100-G109 from open gap to close gap

Page46: change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap

Page46: delete TC19 and change TC20 from DY to GFX

Page49: change G55-G67 G74-G77 from open gap to close gap

Page29: change RN75 from 47ohm to 75ohm

Page28: change C804 C807 from 4.7u to 1u 25V X5R

Page45: delete TC24

Page39: delete L114 L129

12/04

Page24: change U47 from 74.00545.A79 to 74.00547.A79

Page20: swap HDMI signals for routing

Page28: change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R

Page48: change BAT1 from 20.81094.007 to 20.81156.007

Page22: change ODD1 from 62.10065.541 to 62.10065.751

Page22: change R231 R247 from 0ohm resistor to 0ohm pad

12/05

Page25: change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad

Page46: change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request

Page41: change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request

Page41: change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request

Page45: change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request

12/08

Page26: change EC7 from DY to mount EMI's request

Page48: change EC28 EC30 EC31 EC32 from DY to mount EMI's request

Page31: change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request

Page5: change C79 C80 from DY to mount EMI's request

Page46: change C659 from DY to GFX EMI's request

Page50: change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request

Page50: add EC61-EC67 0.1u by EMI's request

Page20: change R313 R314 from 10K 100K to 18K 47K by NV's request

Page35: change U14 pin83 RN65 pin2 from SHEM to DBC_EN by annie's request

Page18: change LCD1 pin35 from NC to DBC_EN by annie's request

Page20: add ER1-ER8 0ohm pad by EMI's request

Page10: change C636 from 1000p DY to 27p mount by RF's request

12/09

Page49: change R406 from 6K2 to 4K75 by power team's request

Page46: change TC16 from mount to GFX

Page50: add TC19 TC24 100u

Page41: change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY

Page46: change C656 C653 from 10u to 4.7u and change C653 from GFX to DY

Page42: change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY

Page41: change TC5 from DY to mount

Page5: change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount

Page17: change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount

Page16: change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount

Page20: change HDMI from 62.10078.161 to 62.10078.171 by CE's request

Page24: change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request

12/10

Page46: add C873 33p GFX by RF's request

Page43: add C874 C875 33p by RF's request

Page20: swap U8 pin13 14 47 48

Page33: change R16 from DY to mount

Page47: change R292 from 0ohm resistor to 0ohm pad

12/11

Page33: change MINI2 pin 51 from 5V_S5_MIN1 to 5V_S5_MIN2

12/15

Page52: change VRAM strap R350

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